Freescale Semiconductor
Technical Data

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MC13224V

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Advanced ZigBee™ - Compliant Platform-in-Package (PiP) for the 2.4 GHz IEEE® 802.15.4 Standard

Package Information
Case 1901-01
99-Pin [9.5X9.5X1.2mm]

Ordering Information

Device	Device Marking	Package
MC13224V[1]	MC13224V	LGA
MC13224VR2[1]	MC13224V	LGA

[1] See Table 1 for more details.

1 Introduction

The MC13224V is Freescale's third-generation ZigBee platform which incorporate a complete, low power, 2.4 GHz radio frequency transceiver, 32-bit ARM7 core based MCU, hardware acceleration for both the IEEE 802.15.4 MAC and AES security, and a full set of MCU peripherals into a 99-pin LGA Platform-in-Package (PiP).

The MC13224V solution can be used for wireless applications ranging from simple proprietary point-to-point connectivity to complete ZigBee mesh networking. The MC13224V is designed to provide a highly integrated, total solution, with premier processing capabilities and very low power consumption.

The MC13224V MCU resources offer superior processing power for ZigBee applications. A full 32-bit ARM7TDMI-S core operates up to 26 MHz. A 128 Kbyte FLASH memory is mirrored into a 96 Kbyte RAM for upper stack and applications software. In addition, an 80 Kbyte ROM is available for boot software, standardized IEEE 802.15.4 MAC and

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communications stack software. A full set of peripherals and Direct Memory Access (DMA) capability for transceiver packet data complement the processor core.

The RF radio interface provides for low cost and the high density as shown in Figure 1. An onboard balun along with a TX/RX switch allows direct connection to a single-ended 50-Ω antenna. The integrated PA provides programmable output power typically from -30 dBm to +4 dBm, and the RX LNA provides -96 dBm sensitivity. In addition, separate complementary PA outputs allow use of an external PA and/or an external LNA for extended range applications. The device also has onboard bypass capacitors and crystal load capacitors for the smallest footprint in the industry. All components are integrated into the package except the crystal and antenna.

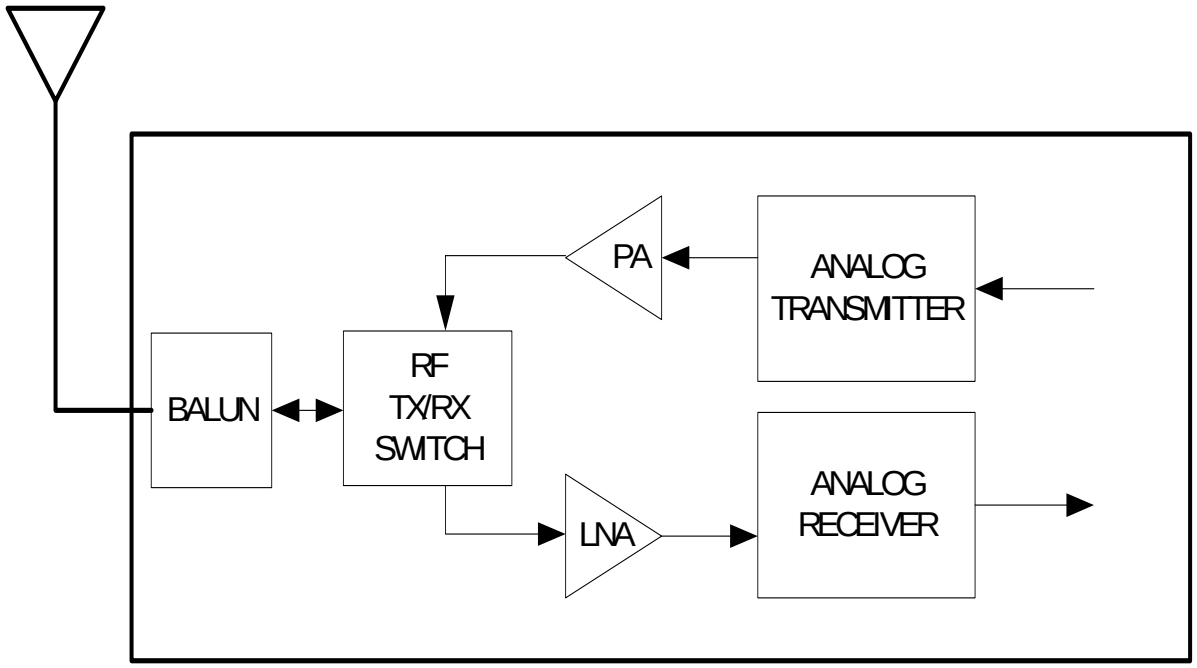


Figure 1. MC13224V RF Radio Interface

In addition to the best-in-class MCU performance and power, the MC13224V also provides best-in-class power savings. Typical transmit current is 29 mA and typical receive current is 22 mA with the CPU at 2 MHz operation and even lower with the bus stealing enabled. Onboard power supply regulation is provided for source voltages from 2.0 Vdc to 3.6 Vdc. Numerous low current modes are available to maximize battery life including sleep or restricted performance operation.

Applications include, but are not limited to, the following:

- Residential and commercial automation
  - — Lighting control
  - — Security
  - — Access control
  - — Heating, ventilation, air-conditioning (HVAC)
  - — Automated meter reading (AMR)
- Industrial Control

  - Asset tracking and monitoring
  - Homeland security
  - Process management
  - Environmental monitoring and control
  - HVAC
  - Automated meter reading
- Health Care
  - Patient monitoring
  - Fitness monitoring
- Consumer
  - Remote control
  - Entertainment systems
  - Cellular phone attach

1.1 Ordering Information

Table 1 provides additional details about the MC13224V

Table 1. Orderable Parts Details

Device	Operating Temp Range (TA.)	Package	Memory Options	Description
MC13224V	-40° to 105° C	LGA	96KB RAM, 128KB Flash	Intended for 802.15.4 Standard compliant applications, Freescale 802.15.4 MAC, and Freescale BeeStack™.
MC13224VR2	-40° to 105° C	LGA Tape and Reel		

2 Features

This section provides a simplified block diagram and highlights MC13224V features.

2.1 Block Diagram

Figure 2 shows a simplified block diagram of the MC13224V.

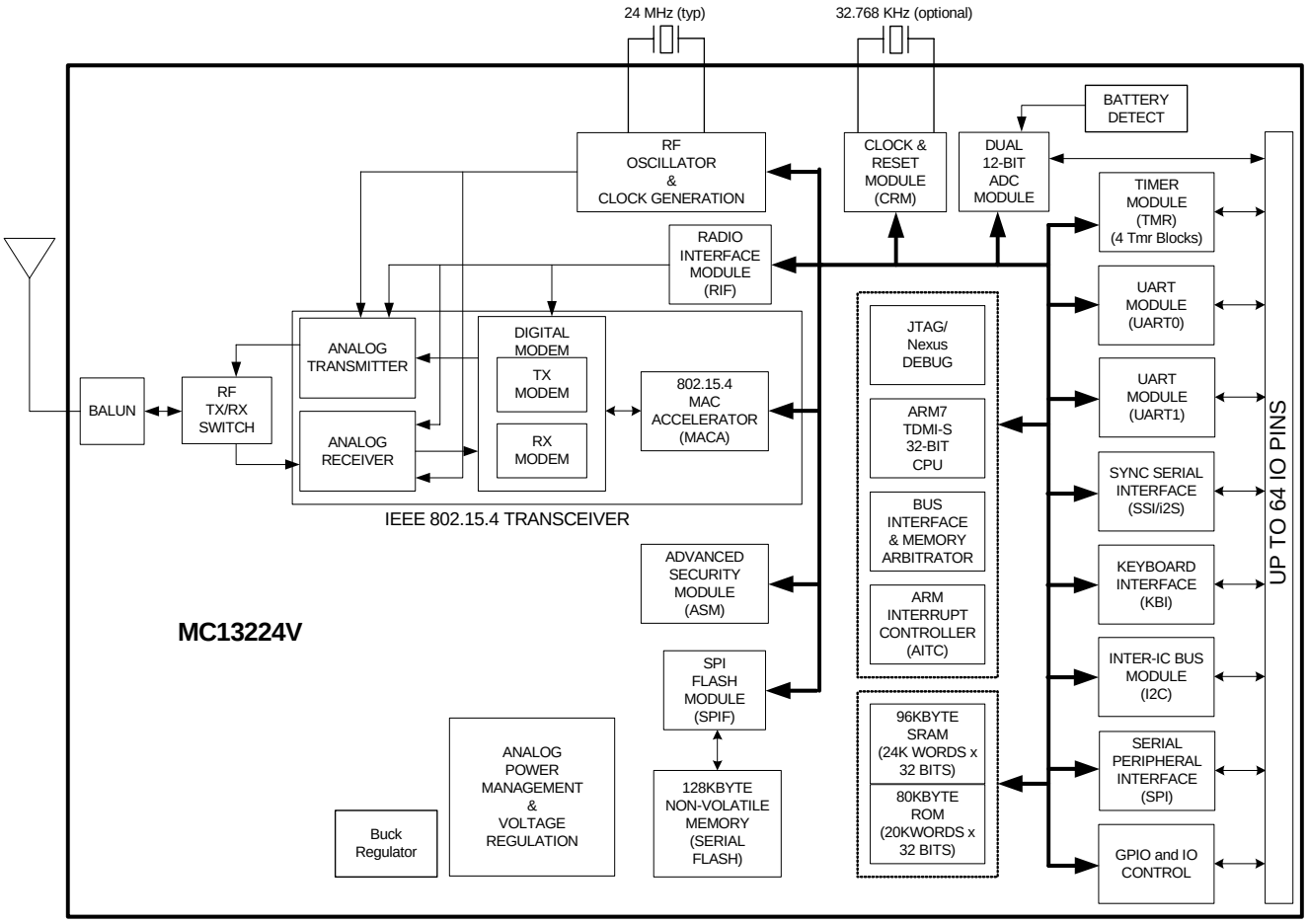


Figure 2. MC13224V Simplified Block Diagram

2.2 Features Summary

- IEEE 802.15.4 standard compliant on-chip transceiver/modem
  - 2.4 GHz ISM Band operation
  - 16 selectable channels
  - Programmable transmitter output power (-30 dBm to +4 dBm typical)
  - World-class receiver sensitivity
    - < -96 dBm typical receiver sensitivity using DCD mode (<1% PER, 20-byte packets)
    - < -100 dBm typical receiver sensitivity using NCD mode (<1% PER, 20-byte packets)
- Hardware acceleration for IEEE 802.15.4 applications
  - MAC accelerator (sequencer and DMA interface)
  - Advanced encryption/decryption hardware engine (AES 128-bit)
- Supports standard IEEE 802.15.4 signaling with 250 kbps data rate
- 32-bit ARM7TDMI-S CPU core with programmable performance up to 26 MHz (24 MHz typical)
- Extensive on-board memory resources
  - 128 Kbyte serial FLASH memory (will be mirrored into RAM)
  - 96 Kbyte SRAM
  - 80 Kbyte ROM
- Best-in-class power dissipation
  - 22 mA typical RX current draw (DCD mode) with radio and MCU active
  - 29 mA typical TX current draw with radio and MCU active (coin cell capable)
  - 3.3 mA typical current draw with MCU active (radio off)
  - 0.8 mA typical current with MCU idle (radio off)
  - 0.85 μA typical Hibernate current (retain 8 Kbyte SRAM contents)
  - 0.4 μA maximum Off current (device in reset)
- Extensive sleep mode control and variation
  - Hibernate and Doze low power modes
  - Programmable degree of power down
  - Clock management
  - Onboard 2 kHz oscillator for wake-up timer.
  - Optional 32.768 kHz crystal oscillator for accurate real-time sleep mode timing and wake-up with a possible sleep period greater than 36.4 hours
  - Wake-up through programmable timer, external real-time interrupts, or ADC timer
- Extensive MCU peripherals set
  - Dedicated 802.15.4 modem/radio interface module (RIF)
  - Dedicated NVM SPI interface for managing FLASH memory
  - Two dedicated UART modules capable of 2 Mbps with CTS/RTS support
  - SPI port with programmable master and slave operation

  - 8-pin keyboard interface (KBI) supports up to a 4x4 matrix. Also, provides up to four asynchronous interrupt inputs for wake-up
  - Two 12-bit analog-to-digital converters (ADCs) share 8 input channels
  - Four independent 16-bit timers with PWM capability. These can cascade in combinations up to 64-bit operation
  - Inter-integrated circuit (I^2C) interface
  - Synchronous Serial Interface (SSI) with I^2S and SPI capability and FIFO data buffering
  - Up to 64 programmable I/O shared by peripherals and GPIO
- Powerful In-circuit debug and FLASH programming available via on-chip debug ports
  - JTAG debug port
  - Nexus extended feature debug port
- System protection features
  - Low battery detect
  - Watchdog timer (COP)
  - Sleep mode timer
- Low external component count
  - Only antenna needed for single-ended 50-Ω RF interface (balun in package)
  - Only a single crystal is required for the main oscillator; programmable crystal load capacitors are on-chip
  - All bypass capacitors in package
- Supports single crystal reference clock source (typical 24 MHz crystal with 13 - 26 MHz usable) with on-chip programmable crystal load capacitance or external frequency source. Also provides onboard 2 kHz oscillator for wake-up timing or an optional 32.768 kHz crystal for accurate low power timing.
- 2.0 V to 3.6 V operating voltage with on-chip voltage regulators.
- Optional buck converter for better battery life.
- -40 °C to +105 °C temperature range
- RoHS-compliant 9.5mm x 9.5mm x 1.2mm 99-pin LGA package

2.3 High Density, Low Component Count, Integrated IEEE 802.15.4 Solution

The MC13224V is more than a high performance, low power platform-in-a-package IEEE 802.15.4 solution. Not only are the transceiver (radio) and MCU on an SoC, the packaged solution contains a 128 Kbyte serial FLASH memory, onboard bypass capacitors for critical nodes, and RF components that present a single-ended 50-Ω interface for an external antenna. The radio is a full differential design with an on-chip transmit/receive (TX/RX) switch, and the PiP also has an onboard balun for differential to singled-ended conversion. On-chip RF matching is also provided to present the proper impedance to the antenna.

To further simplify the application, single crystal operation (optimized for 24 MHz) is supported for full radio and MCU operation. If the default 24 MHz crystal is not used, the device supports 13-26 MHz crystals also. The load capacitance to the crystal oscillator is supplied on-chip to eliminate the need for the otherwise required external capacitors.

2.4 Integrated IEEE 802.15.4 Transceiver (Radio and Modem)

The MC13224V IEEE 802.15.4 fully-compliant transceiver provides a complete 2.4 GHz radio with 250 kbps Offset-Quadrature Phase Shift Keying (O-QPSK) data in 5.0 MHz channels and full spread-spectrum encode and decode. The modem supports transmit, receive, clear channel assessment (CCA), Energy Detect (ED), and Link Quality Indication (LQI) as required by the 802.15.4 Standard.

2.4.1 RF Interface and Usage

The MC13224V RF interface provides for a single-ended, 50-Ω port that connects directly to an antenna. There is an onboard balun that converts the single-ended interface to a full differential, bi-directional, on-chip interface with transmit/receive switch, LNA, and complementary PA outputs. The required port impedance matching is also onboard. This combination allows for a very small footprint and a very low cost RF solution.

The receiver demodulator includes a module called the Differential Chip Detector which has two modes of operation:

- Non-coherent Detection (NCD) with automatic frequency control (AFC)
- Non-coherent Differential Chip Detection (DCD) without AFC

The IEEE 802.15.4 standard allows a maximum clock drift of ±40 ppm (which equals ±80 ppm station-to-station). The MC13224V 802.15.4 demodulator includes two different methods of operating in the presence of such large frequency errors:

NCD Mode	Provides an increased ~3.5 dB of sensitivity. However, the addition of the AFC increases the demodulator current drain about 3 mA.
DCD Mode	Default receive mode at lower current.

For longer range applications where external amplification may be desired (LNA and/or PA), additional ports are provided for secondary complementary PA outputs. These can be used as a separate PA interface while the single-ended port through the balun is used as an input only. Also, four control pins and a

regulated 20mA voltage source are provided to control external components and supply power to the PA outputs.

The RF Interface functionality can be summarized as follows:

- Programmable output power — 0 dBm nominal output power, programmable from -30 to +4 dBm
- Receive sensitivity (at 1% PER, 20-byte packet) -
  - — < -96 dBm (typical) DCD receive (well above IEEE 802.15.4 specification of -85 dBm)
  - — < -100 dBm (typical) NCD receive (higher current)
- Single-ended 50-Ω antenna port — Uses integrated transmit/receive (T/R) switch, LNA, and onboard balun. Impedance matching onboard.
- Maximum flexibility — The optional single-ended port becomes RF input only and a separate set of full differential PA outputs are provided. Separate input and outputs allow for a variety of RF configurations including external LNA and PA for increased range
- Four control signals for external RF components such as a LNA or PA
- Regulated voltage source for PA biasing and powering external components

2.4.2 Modem

The modem supports the full requirement of the IEEE 802.15.4 Standard to transmit and receive data packets. In additional, the mechanism is present to measure received signal level to provide CCA, ED, and LQI as required by the 802.15.4 Standard.

2.5 High Performance, Low Power 32-Bit ARM7 Processor

- The ARM7TDMI-S processor is a member of the 32-bit ARM family of general-purpose 32-bit microprocessors that offers high performance with very low-power consumption
- A three stage instruction pipeline (fetch, decode, execute) increases the speed of the flow of instructions to the processor
- Data access can be 8-bit bytes, 16-bit half words, or 32-bit words. Words must be aligned to 4-byte boundaries. Half words must be aligned to 2-byte boundaries
- The ARM7TDMI-S processor supports two instruction sets, the 32-bit ARM instruction set and the 16-bit Thumb instruction set. The Thumb mode incorporates 16-bit instructions for higher code density while retaining all the benefits of a 32-bit architecture, such as the full 32-bit registers, 32-bit operations, and 32-bit memory transfer. The use of the instruction sets can be intermixed for maximizing performance while retaining higher code density

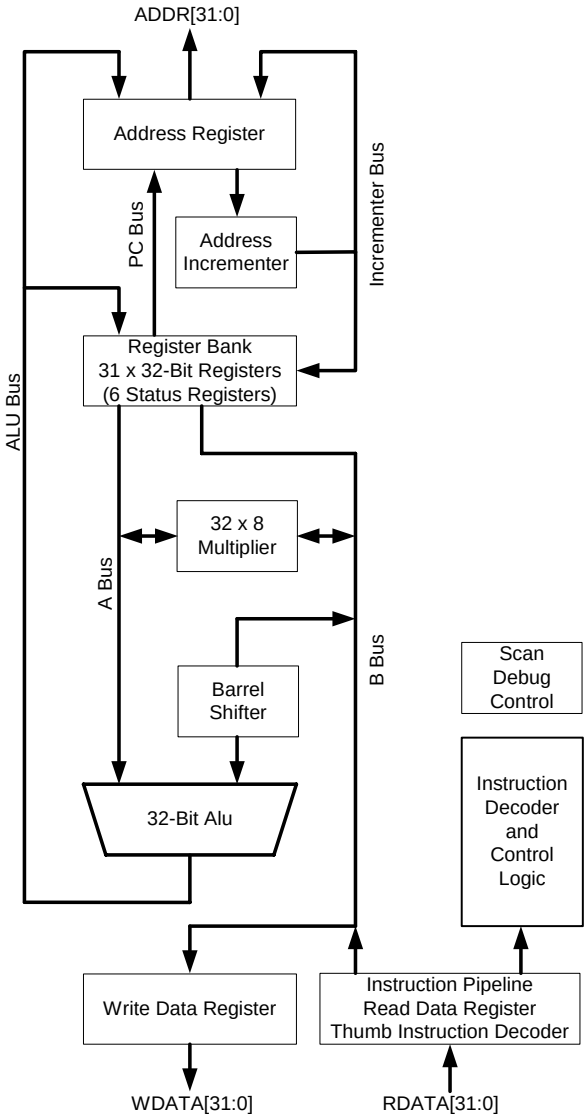


Figure 3. ARM7TDMI-S 32-Bit CPU Core

2.6 Low Power Operation and Power Management

The MC13224V is inherently a very low power device, but it also has extensive power management and an onboard buck regulator option to maximize battery life.

2.6.1 Operating Current

The MC13224V operating currents are a function of operating mode. There are two basic low power modes of Hibernate and Doze, and both have options of how much RAM contents are retained. The difference between Hibernate and Doze is that Doze mode keeps the primary reference oscillator running.

Highest operating current is when the radio is active for transmit or receive. Refer to Section 6.4, “Supply Current Characteristics” for more details and specifications.

2.6.2 Power Management

The MC13224V power management is controlled through the Clock and Reset Module (CRM). The CRM is a dedicated module to handle MCU clock, reset, and power management functions which includes control of the power regulators. All these functions have impact on attaining lowest power.

2.6.2.1 CRM Features

The CRM features include:

- Control of system reset
- Control clock gating for power savings
- Sleep mode (Hibernate and Doze) management
  - — Degree of chip power down
  - — Retention of programmed parameters
  - — Programmable retention of RAM contents
  - — Clock management
- Wake-up management
  - — Graceful power-up
  - — Clock management
  - — Wake-up via programmable timer or external interrupts.
- Wake-up timer
  - — Hibernate mode - based on onboard 2 kHz oscillator or optional 32.768 kHz crystal oscillator
  - — Doze mode - based on main reference oscillator, typically 24 MHz
- Controls reference clocks based on default 24 MHz crystal oscillator or optional 13-26 MHz oscillator with PLL (external filter) for 24 MHz frequency synthesis.
- MCU watchdog timer (COP)
- Software initiated reset
- Management control of onboard linear regulators and optional buck regulator

2.6.2.2 CRM Operation

The CRM has primary control of the entire system:

- Reset and power up — After release of the hardware RESETB signal, the CRM will perform a power up sequence of the MCU. The linear regulators and clock sources are managed for a graceful start-up of the MCU and its resources. The radio is not powered until needed
- Normal operation of MCU — The clock management of the MCU and its resources are controlled by the CRM. The processor clock is programmable from low frequencies up to the maximum reference frequency (13-26 MHz optional w/24 MHz standard) to allow the application to trade-off processing speed versus power savings
- Sleep modes and recovery — There are two sleep modes of Hibernate and Doze. The primary difference is that Doze mode keeps the reference oscillator running. Both modes can retain critical

programmed parameters and have selectable sizes of RAM retention. Hibernate has lowest power, but Doze allows high accuracy sleep timing. The CRM manages the recovery from low power, similar to power-up from reset, providing regulator and clock management.

— Wake-up can be based on external interrupts through 4 KBI inputs

— Wake-up can be from internal interrupts

— Wake-up can be based on an RTI (wake-up) timer.

- The RTI timer has two possible frequency sources that provide a very low power wake-up option from sleep
  — One option is an onboard, low accuracy 2 kHz oscillator
  — A second option is to add an external 32.768 kHz crystal for the RTI clock source
  — A 32-bit timer allows greater than a 36.4 hour wake-up delay with the 32.768 crystal oscillator
- Other features of the CRM:
  — An optional COP watchdog timer to monitor CPU program activity
  — A programmable software reset

2.6.3 Optional Buck Regulator

For battery based applications, an optional buck regulator is provided to maximize battery life. Figure 4 shows the configuration of the buck regulator versus the normal connection. An onboard MOSFET is used as a switch with an external 100µH inductor and 10µF capacitor when the buck regulator is enabled.

The buck regulator drops the higher battery voltage to 1.8 - 2.0 Vdc that is applied to the onboard linear regulators. This allows lower net current from the battery to maximize the life of the battery.

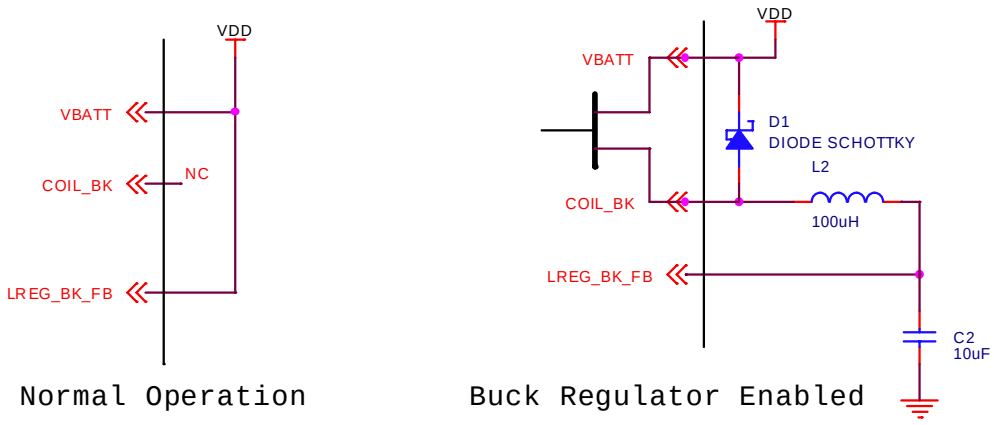


Figure 4. Optional Buck Regulator

2.6.4 Battery Detect

An optional feature of the ADC module is battery voltage detect. Programmable thresholds are provided for an ADC analog sample channel to monitor the battery high voltage and battery low voltage. This feature can be used as a trigger to provide low battery indication, protection for data that may be lost due to end-of-life for the battery, monitoring charging, and controlling buck regulator operation.

2.7 IEEE 802.15.4 Acceleration Hardware

The MC13224V provides acceleration hardware for IEEE 802.15.4 applications and this hardware includes 802.15.4 MAC acceleration and AES encryption/decryption.

2.7.1 802.15.4 MAC Accelerator (MACA) Overview

The MC13224V contains a hardware block that provides a low-level MAC and PHY link controller, which together with software running on the ARM core, implements the baseband protocols and other low-level link routine control and link control. Components of the MACA include a sequencer/controller (with timers), TX and RX packet buffers, DMA block, frame check sequence (FCS) generator/checker, and control registers. Figure 5 shows a MACA simplified block diagram.

As part of the 802.15.4 protocol, packets are generated and transmitted, packets are received and verified, and channel energy is measured via a clear channel assessment (CCA). Also, combinations or sequences of events are required as part of the protocol such as an ACK response following a received packet. The MACA facilitates these activities via control of the transceiver and off loads the functions from the CPU. A dedicated DMA function moves data between the MACA buffers and RAM on a cycle steal basis and does not require intervention from the CPU.

The MACA is responsible for construction of packets for TX including FCS, and for parsing the received packets. The MACA will also handle ACKs and TxPoll sequences independent of the ARM processor. During TX the MACA will construct the entire packet. This includes preamble and SFD (start of frame delimiter). During receive, the modem will recognize preamble and SFD, then the MACA will begin receiving the packet with the first bit of frame length, and finally, will check the FCS.

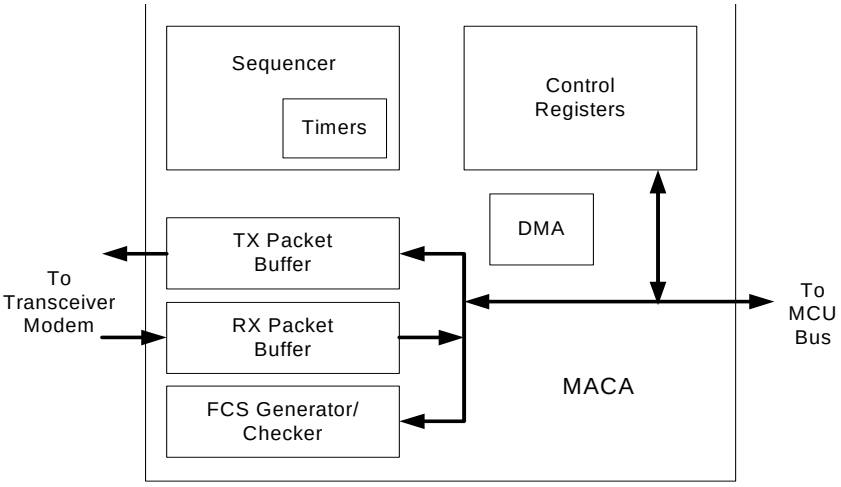


Figure 5. MAC Accelerator Simplified Block Diagram

NOTE

The radio can receive packets of either mode without prior indication of the incoming packet mode.

2.7.1.1 MACA Features

In order to reduce CPU load, the MACA module has embedded features for controlling parts of the IEEE 802.15.4 PHY and MAC layer requirements. The MACA core features include:

- Sequence Manager sequences / auto sequences
  - RX only
  - TX only
  - Automatic acknowledgment frame reception on transmitted packets
  - Automatic acknowledgment frame transmission on received packets
  - Auto-RX for continuous reception as coordinator
  - Auto sequence for transmitted MAC data.request
  - Assist for efficient response to MAC data.request
  - Embedded channel assessment in sequence
  - Support for sequences with slotted mode access
  - Timer triggered and immediately executed actions
  - Support for extended RX for reception in random backoff and battery life extension
  - Support for promiscuous mode
- Programmable auto sequence timing - Each CCA, RX, or TX event is an independent operation. The radio gets through a power-up or “warm-up” sequence for each operation (including VCO), and there is also a power-down or “warm-down” time. Sequences are combinations of radio operations and are highly configurable.
  - RX warm-up is 72 µs
  - TX warm-up is 92 µs
  - Turnaround times
    - The IEEE 802.15.4 Standard requires a TX-to-RX or a RX-to-TX turnaround time to be less than or equal to 12 symbols times (192 µs).
    - Best practice for maximum station-to-station performance is to minimize TX-to-RX turnaround time and to maximize (within spec) RX-to-TX turnaround time.
    - Auto sequences should use recommended turnaround times of:
      a) 11 symbols times (176 µs) RX-to-TX
      b) 96 µs TX-to-RX.
- Dedicated DMA for transfer of TX/RX data from/to RAM (minimum bus clock of 2 MHz for 802.15.4 modem operation)
- Maskable, event-driven interrupt generation
- Address header filtering for received packets. A promiscuous mode allows bypass of the filtering for monitoring network traffic
- Packet manager
  - Handles preamble data
  - Handles frame check sequence (FCS) a.k.a CRC

— Embedded header filter for received packets

- Beacon Support Mode
- Control/status registers mapped into CPU memory map
- 32-Bit random number generator — Runs at the bus clock rate, a 32-bit Linear Feedback Shift Register (LFSR) can be set with a seed value and uses a 32-bit primitive polynomial. A 32-bit random number is fetched with every read of the proper control register

2.7.2 Advanced Security Module (ASM)

The IEEE 802.15.4 Standard and the ZigBee Standard both provide for optional use of data encryption.The ASM engine is a hardware block that accelerates encryption/decryption using the Advanced Encryption Standard (AES). The engine can perform “Counter” (CTR) and Cipher Block Chaining (CBC) encryption. The combination of these two modes of encryption are known as CCM mode encryption. CCM is short for Counter with CBC-MAC. CCM is a generic authenticate and encrypt block cipher mode. CCM is only defined for use with 128 bit block ciphers, such as AES. The definition of CCM mode encryption is documented in the NIST publication SP800-38C.

The ASM has the following features:

- 32-Bit wide bus interface
- CTR encryption in 13 clock cycles
- CBC encryption in 13 clock cycles
- Encrypts 128 bits as a unit
- The 128-bit registers are aligned on quad word boundaries (16 byte)
- Self-test mode
- Maskable “action complete” interrupt

3 Memory

The MC13224V memory resources consist of RAM, ROM, and serial FLASH.

3.1 RAM and ROM

The RAM and ROM features include:

- 96 Kbytes RAM.
  - RAM0: 8 Kbytes, 2 Kwords (2048 x 32 bits)
  - RAM1: 24 Kbytes, 6 Kwords (6144 x 32 bits)
  - RAM2: 32 Kbytes, 8 Kwords (8192 x 32 bits)
  - RAM3: 32 Kbytes, 8 Kwords (8192 x 32 bits)
- All read or write accesses require a minimum of two system clock cycles
- Stall signal generated for read after write cycles
- Clock is enabled only on the accessed memory device for low power consumption
- RAMs have been divided to allow for power savings. While sleeping, the above RAM blocks can be turned off (combinations include 8, 32, 64, and 96 Kbytes active) and the RAM remainder can be placed in a low voltage mode for data retention. If more RAMs are turned on, then less battery life will be achieved. Depending on the amount of RAM powered during sleep, the boot time may be longer with less RAM as the non-powered RAM must be reloaded from FLASH.
- 80 Kbytes ROM
  - 20 Kwords (20480 x 32 bits)
  - Initially contains bootstrap code, 802.15.4 MAC (no security), UART driver, and SPI driver. The MAC software builds on the lower level hardware capability of the transceiver and MACA. All code except the bootstrap is “patchable”.
  - Can be extended later to communications stack software and NVM services (erase, program, and read routines)

3.2 Serial FLASH (NVM)

The MC13224V also contains a 128 Kbyte serial FLASH memory that can be mirrored into the 96 Kbyte RAM. The serial FLASH is accessed via an internal dedicated SPI module (SPIF). The FLASH erase, program, and read capability are programmed through the SPIF port. The FLASH is accessed at boot time to load/initialize RAM. All actual CPU program and data access is from RAM or ROM.

4 MCU Peripherals

The MC13224V has a rich set of MCU peripherals. Figure 6 shows the peripheral modules.

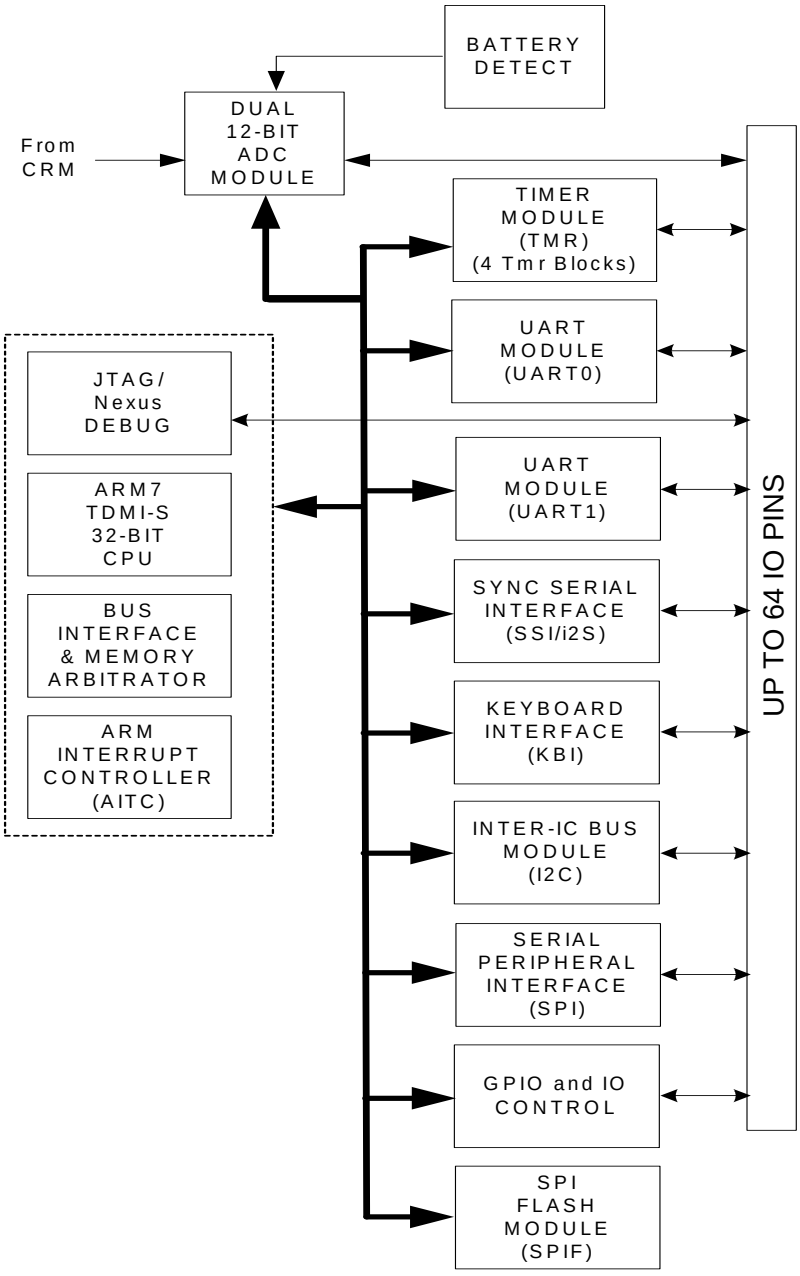


Figure 6. MCU Peripherals

4.1 Parallel IO (GPIO)

The parallel I/O features include:

- A total of 64 general-purpose I/O pins
- Individual control (direction and output state) for each pin when in GPIO mode
- Pad hysteresis enables
- Software-controlled pull-ups/pull-downs on each input pin
- When not used as GPIO, the IO provide alternative functions
  - Debug ports for JTAG (four signals) and Nexus (fourteen signals) modules
  - Four control signals for external RF components such as an LNA, PA, and antenna switch
  - Eight analog inputs for ADC input channels
  - Four signals for ADC reference voltages
  - Eight signals for UART1 and UART2
  - Two I^2C signals
  - Four timer block signals
  - Four SPI block signals
  - Four SSI block signals
  - Eight KBI signals
- Eight KBI pins are kept alive during Hibernate or Doze. Four KBI are output and four are inputs. The input can be used as wake-up interrupts

4.2 Keyboard Interface (KBI)

The MC13224V designates 8 pins (KBI_0 to KBI_7) as a keyboard interface, where four of these signals typically are outputs and four are inputs (KBI_4 to KBI_7) that support interrupts. These 8 pins could typically be used as a matrix interface to support up to 16 switches or buttons, such as a keypad. These signals can also be used as general purpose IO if a keyboard is not present.

During Hibernate or Doze, the KBI are unique in that they are kept alive. Four KBI are outputs and four KBI are inputs. The inputs can be enabled as asynchronous interrupts to wake-up the MC13224V from the sleep mode.

4.3 Timer (TMR) Module

The MC13224V provides a timer module (TMR) that contains four identical counter/timer groups. Each group is capable of many variants of input capture, output compare and pulse-width modulation. The wide range of operational modes is useful for many control and sensor applications.

Figure 7 shows a block diagram of an individual timer group.

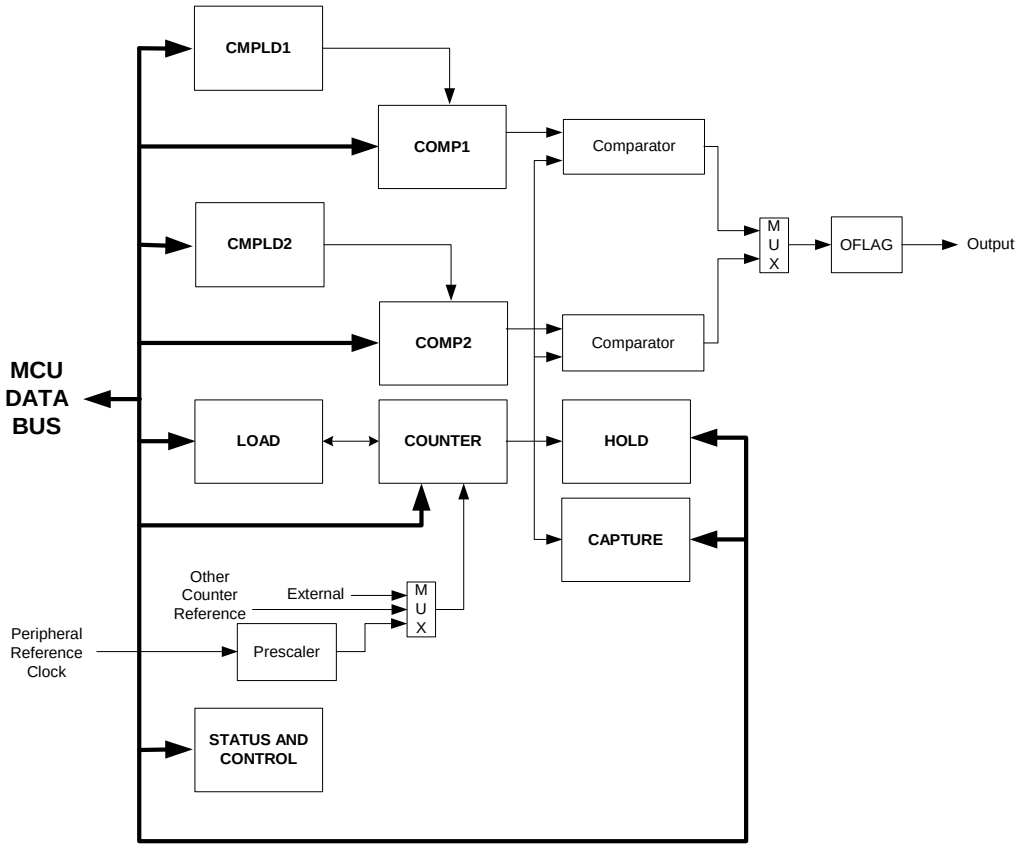


Figure 7. Timer Group Block Diagram

Each 16-bit counter/timer group contains a prescaler, a counter, a load register, a hold register, a capture register, two compare registers, and status and control registers.

- Load Register — Provides the initialization value to the counter when the counter's terminal value has been reached
- Hold Register — Captures the counter's value when other counters are being read. This feature supports the reading of cascaded counters
- Capture Register — Enables an external signal to take a snap shot of the counter's current value
- COMP1 and COMP2 Registers — Provides the values to which the counter is compared. If a match occurs, the OFLAG signal can be set, cleared, or toggled. At match time, an interrupt is generated (if enabled), and the new compare value is loaded into the COMP1 or COMP2 registers from CMPLD1 and CMPLD2 if enabled
- The Prescaler provides different time bases useful for clocking the counter/timer

- The Counter provides the ability to count internal or external events
- Control and Status Registers — Provides operational mode control of the counter, status, clock source control, interrupt control, and external interface control

Four GPIO pins (TMR0 -TMR3) are programmable and can be used with any counter/timer group.

The TMR module feature include:

- Four 16-bit counters/timers groups
- Up/down count
- Counters are cascadable for up to 64 bit delay counter
- Programmable count modulo.
- Peripheral reference clock equates to reference oscillator frequency
- External clock max count rate equals peripheral clock divided by 2
- Internal clock max count rate equals peripheral clock.
- Count once or repeatedly
- Counters are preloadable
- Compare registers are preloadable
- Counters share available four GPIO pins (programmable as inputs or outputs and programmable for falling or rising edge)
- Separate prescaler for each counter
- Each counter has capture and compare capability
- Optional input glitch filter
- Functional modes include stop, count, edge-count, gated-count, quadrature-count, signed-count, triggered-count, one-shot, cascade-count, pulse-output, fixed frequency PWM, and variable-frequency PWM

4.4 UART Modules

The MC13224V has two universal asynchronous receiver/transmitter (UART) modules. Each UART has an independent fractional divider, baud rate generator that is clocked by the peripheral bus clock (typically 24 MHz) which enables a broad range of baud rates up to 1,843.2 kbaud. Transmit and receive use a common baud rate for each module.

Each UART provides the following features:

- 8-bit only data
- One or two stop bits
- Programmable parity (even, odd, and none)
- Four-wire serial interface (RXD, TXD, RTS, and CTS)
- Hardware flow control support for RTS and CTS signals
- 32-byte receive FIFO and 32-byte transmit FIFO
- Programmable sense for RTS/CTS pins (high true/low true)

- Status flags for various flow control and FIFO states
- Receiver detects framing errors, start bit error, break characters, parity errors, and overrun errors.
- Voting logic for improved noise immunity (16X/8X oversampling)
- Maskable interrupt request
- Time-out counter, which times out after eight non-present characters
- Receiver and transmitter enable/disable
- Low-power modes
- Baud rate generator to provide any multiple-of-2 baud rate between 1.2 kbaud and 1,843.2 kbaud

4.5 Inter-Integrated Circuit (I^2C) Module

The MC13224V provides an Inter-Integrated Circuit (I^2C) module for the I^2C which is a two-wire, serial data (SDA) and serial clock (SCL), bidirectional serial bus. The I^2C allows for data exchange between the MC13224V and other devices such as MCUs, serial EEPROM, serial ADC and DAC devices, and LCDs. The I^2C minimizes interconnections between devices and is a synchronous, multi-master bus that allows additional devices to be connected and still handle system expansion and development. The bus includes collision detection and arbitration to prevent data corruption if two or more masters attempt to simultaneously control the I^2C.

The I^2C module is driven by the peripheral bus clock (typically 24 MHz) and the SCL bit clock is generated from a prescaler. The prescaler divide ratio can be programmed from 61,440 to 160 (decimal) which gives a maximum bit clock of 150 kbps.

The I^2C module supports the following features:

- Two-wire (SDA and SCL) interface
- Multi-master operation
- Master or slave mode
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation/detection
- Acknowledge bit generation/detection
- Bus busy detection
- Software-programmable bit clock frequency up to 150 kbps
- Software-selectable acknowledge bit
- On-chip filtering for spikes on the bus

4.6 Serial Peripheral Interface (SPI) Modules

The MC13224V has two SPI modules that use a common architecture

4.6.1 External SPI Module

The MC13224V offers a dedicated Serial Peripheral Interface (SPI) module for external use. The SPI is a high-speed synchronous serial data input/output port used for interfacing with serial memories, peripheral devices, or other processors. The SPI allows a serial bit stream of a programmed length (1 to 32 bits) to be shifted simultaneously into and out of the device at a programmed bit-transfer rate (called 4-wire mode). There are four pins associated with the SPI port (SPI_SCK, SPI_MOSI, SPI_MISO, and SPI_SS).

The SPI module can be programmed for master or slave operation. It also supports a 3-wire mode where for master mode the MOSI becomes MOMI, a bidirectional data pin, and for slave mode the MISO becomes SISO, a bidirectional data pin. In 3-wire mode, data is only transferred in one direction at a time.

The SPI bit clock is derived from the peripheral reference clock (typically 24 MHz with a maximum of 26 MHz). A prescaler divides the peripheral reference clock with a programmed divide ratio from 2 to 256. Typical bit clock range will be from 12 MHz to 93.75 kHz.

The SPI has the following features:

- Master or slave mode operation
- Data buffer is 4 bytes (32 bits) in length
- SPI transfer length programmable from 1 to 32 bits
- MSB-first shifting
- Programmable transmit bit rate (typically 12 MHz max)
- Serial clock phase and polarity options
- Full-duplex (4-wire) or bidirectional data (3-wire) operation
- SPI transaction can be polled or interrupt driven
- Slave select signal
- Low Power (SPI Master uses gated clocks. SPI Slave clock derived completely from SPI_SCK.)

4.6.2 SPI FLASH Module (SPIF)

The SPIF is an internal SPI block dedicated to control, reading, and writing of the serial FLASH memory (NVM). It uses the same architecture as the general SPI block, but is limited by the characteristics of the FLASH SPI interface.

4.7 Synchronous Serial Interface (SSI) Module

The MC13224V provides a versatile Synchronous Serial Interface (SSI) which is a full-duplex, serial port that allows communication with a variety of serial devices. These serial devices can be digital signal processors (DSPs), MCUs, peripherals, popular industry audio CODECs, and devices that implement the Inter-Integrated Circuit sound bus standard (I^2S).

The SSI typically transfers samples in a periodic manner and it consists of independent transmitter and receiver sections with common clock generation and frame synchronization. The external signals include the bit clock (SSI_BITCK), frame sync (SSI_FSYN), RX data (SSI_RX), and TX data (SSI_TX). The SSI has the following basic operating modes all with synchronous protocol:

- Normal mode — The simplest SSI mode transfers data in one time slot per frame
- Network mode — Creates a Time Division Multiplexed (TDM) network, such as a TDM CODEC network or a network of DSPs
- Gated Clock mode — Connects to SPI-type interfaces on MCUs or external peripheral chips

With its multi-modes, the SSI can be programmed for two very useful functions:

- A second SPI port augmenting the MC13224V SPI module
- I^2S interface - the SSI is capable of generating the required clock frequencies and data format to drive a serial stereo audio DAC

The SSI includes the following features:

- Synchronous transmit and receive sections with shared internal/external clocks and frame syncs, operating in Master or Slave mode.
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as thirty-two time slots
- Gated Clock mode operation requiring no frame sync
- SSI clock source is Peripheral Clock (typically 24 MHz); maximum SSI transfer rate is 6.0 MHz
- Separate Transmit and Receive FIFOs. Each of which is 8x24 bits
- Programmable data interface modes including I^2S, LSB, MSB aligned
- Programmable word length (8, 10, 12, 16, 18, 20, 22 or 24 bits)
- Program options for frame sync and clock generation
- Programmable I^2S modes (Master, Slave)
- Programmable internal clock divider
- Time Slot Mask Registers for reduced CPU overhead (for Tx and Rx both)
- SSI power-down feature

4.8 Analog-to-Digital Converter (ADC) Module

The MC13224V ADC module provides two 12-bit analog-to-digital converters (ADC_1 and ADC_2) with eight external channels (ADC7 - ADC0) that can be multiplexed to either ADC. ADC_1 can also sample a battery reference voltage for monitoring purposes. External pins (ADC2_VREFH, ADC2_VREFL, ADC1_VREFH, and ADC1_VREFL) are provided for independent ADC reference voltages. The minimum sample time is 20 µs. Figure 8 shows a block diagram of the ADC module.

Each ADC can be programmed to scan multiple selected channels on a timed basis. The primary clock to the ADC module is the peripheral reference clock (typically 24 MHz). For the time period between scan sequences, the primary clock is first divided by an 8-bit prescale (1-255), and the derived clock drives both the 32-bit delay timer and the ADC sequencer. Each ADC has its own delay timer and sequencer.

Once a scan sequence has been initiated, all selected channels can be sampled. Registers are provided to define thresholds that can be enabled for the sampled channels. A threshold can be assigned to a specific channel and can be programmed to be a less-than or greater-than threshold. Multiple thresholds can be assigned to a single channel. Warm-up of the analog portion of the ADC circuitry is provided for power management, and a separate 300 kHz ADC clock must be programmed via its own divider.

The battery monitor has two (2) dedicated threshold registers to set the high and low limits of the battery sample channel.

Sample values are stored in a 8x16-bit FIFO. The FIFO accumulates samples from both ADCs, and the 12-bit sample value and a 4-bit channel tag are saved for each sample. The FIFO is read by the CPU from a register address.

The module can be programmed to interrupt the processor based on the timed sample activity. Sample activity, sequencer activity, or FIFO “fullness” can all be enabled to generate an interrupt.

The ADCs can also be overridden to sample on command as opposed to sequencer, time-based activity.

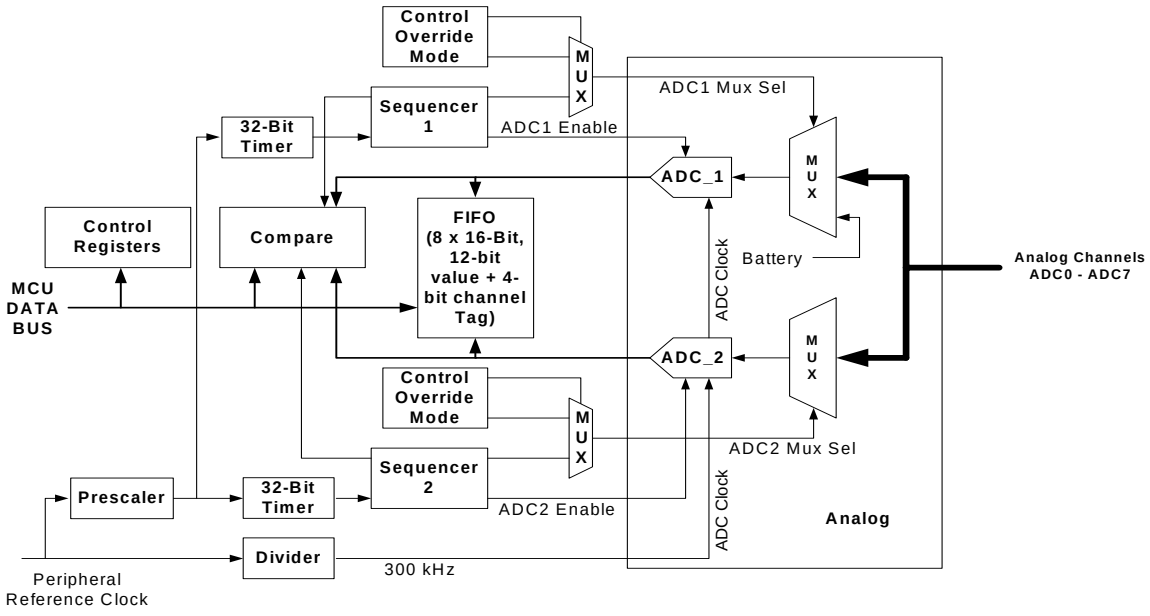
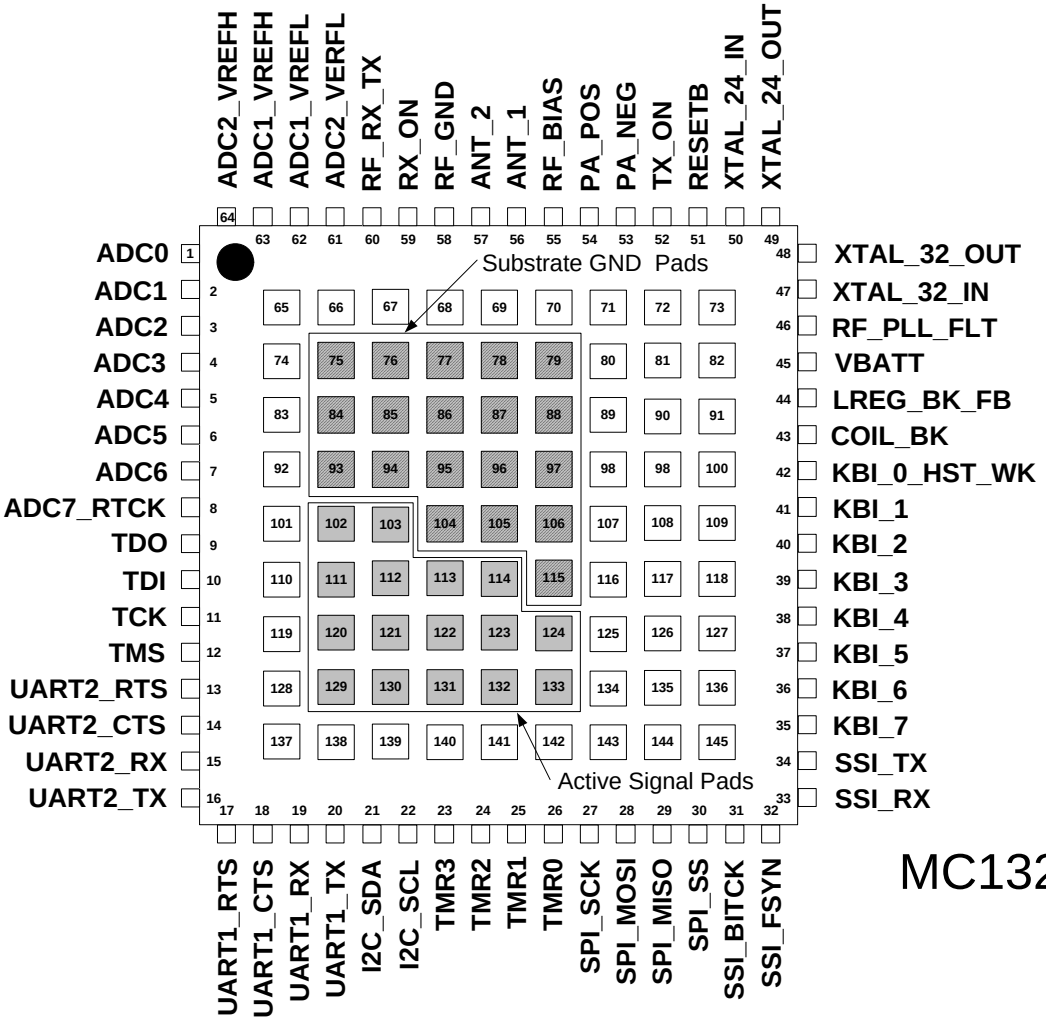


Figure 8. ADC Module Block Diagram

The ADC module has the following features:

- 12 bit resolution. Effective number of bits 8-9
- Valid usable input voltage range: [Vref_high-0.2V] to [Vref_low+0.2V]
- Maximum input range: VBATT to VSS
- Minimum sample time 20 µs
- Peripheral Clock (set by CRM) uses an 8-bit prescaler to provide the time base for the module
- Two independent channels, each with a 32-bit timer
- ADC_1 has 9 channels: 8 external analog inputs plus battery reference voltage
- ADC_2 has 8 channels: 8 external analog inputs
- Active channels for each ADC are programmable
- Eight active monitors plus battery reference monitors can generate a IRQ
- An 8-deep FIFO for recording data
- IRQs can be generated by the channel compare values, FIFO status, and sequencers

5 Pin Assignments and Connections



Notes:

1. **Bottom pads 75-79, 84-88, 93-97, 104-106, and 115 are Substrate Ground.**
2. **Bottom pads 102-103, 111-114, 120-124, and 129-133 are active pads.**
3. **All remaining bottom pads are isolated from ground (NC), and are provided here for mechanical strength.**
4. **Figure 15 (Mechanical Diagram), is the bottom view, not the top view as shown here.**

Figure 9. MC13224V Pinout (Top View: Bottom Pads Shown)

5.1 Pin Definitions

Table 2 details the MC13224V pinout and functionality.

Table 2. Pin Function Description

Pin #	Pin Name	Type	Description[1]	Functionality
1	ADC0	Analog Input or Digital Input/Output	ADC analog input Channel 0 / GPIO30	ADC sample channel can be used by either ADC_1 or ADC_2.
2	ADC1	Analog Input or Digital Input/Output	ADC analog input Channel 1/ GPIO31	ADC sample channel can be used by either ADC_1 or ADC_2.
3	ADC2	Analog Input or Digital Input/Output	ADC analog input Channel 2/ GPIO32	ADC sample channel can be used by either ADC_1 or ADC_2.
4	ADC3	Analog Input or Digital Input/Output	ADC analog input Channel 3/ GPIO33	ADC sample channel can be used by either ADC_1 or ADC_2.
5	ADC4	Analog Input or Digital Input/Output	ADC analog input Channel 4/ GPIO34	ADC sample channel can be used by either ADC_1 or ADC_2.
6	ADC5	Analog Input or Digital Input/Output	ADC analog input Channel 5/ GPIO35	ADC sample channel can be used by either ADC_1 or ADC_2.
7	ADC6	Analog Input or Digital Input/Output	ADC analog input Channel 6/ GPIO36	ADC sample channel can be used by either ADC_1 or ADC_2.
8	ADC7_RTCK	Analog Input or Digital Input/Output	ADC analog input Channel 7 / ReTurn ClocK / GPIO37	ADC sample channel can be used by either ADC_1 or ADC_2. Alternately, the signal returns TCK for JTAG to support adaptive clocking.
9	TDO	Digital Input/Output	JTAG Test Data Output / GPIO49	JTAG debug port serial data output.
10	TDI	Digital Input/Output	JTAG Test Data Input / GPIO48	JTAG debug port serial data input.
11	TCK	Digital Input/Output	JTAG Test Clock Input / GPIO47	JTAG debug port clock input.
12	TMS	Digital Input/Output	JTAG Test Mode Select Input / GPIO46	JTAG debug port test mode select input.
13	UART2_RTS	Digital Input/Output	UART2 Request to Send input / GPIO21	UART2 RTS control input.
14	UART2_CTS	Digital Input/Output	UART2 Clear to Send output / GPIO20	UART2 CTS control output.
15	UART2_RX	Digital Input/Output	UART2 RX data input / GPIO19	UART2 receive data input.

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description[1]	Functionality
16	UART2_TX	Digital Input/Output	UART2 TX data output / GPIO18	UART2 transmit data output.
17	UART1_RTS	Digital Input/Output	UART1 Request to Send input / GPIO17	UART1 RTS control input.
18	UART1_CTS	Digital Input/Output	UART1 Clear to Send output / GPIO16	UART1 CTS control output.
19	UART1_RX	Digital Input/Output	UART1 RX data input / GPIO15	UART1 receive data input.
20	UART1_TX	Digital Input/Output	UART1 TX data output / GPIO14	UART1 transmit data output.
21	I2C_SDA	Digital Input/Output	I^2C Bus data / GPIO13	I^2C bus signal SDA
22	I2C_SCL	Digital Input/Output	I^2C Bus clock / GPIO12	I^2C bus signal SCL
23	TMR3	Digital Input/Output	Timer 3 IO signal / GPIO11	Pin is used as counter output or counter input clock.
24	TMR2	Digital Input/Output	Timer 2 IO signal / GPIO10	Pin is used as counter output or counter input clock.
25	TMR1	Digital Input/Output	Timer 1 IO signal / GPIO9	Pin is used as counter output or counter input clock.
26	TMR0	Digital Input/Output	Timer 0 IO signal / GPIO8	Pin is used as counter output or counter input clock.
27	SPI_SCK	Digital Input/Output	SPI Port clock / GPIO7	SPI port clock.
28	SPI_MOSI	Digital Input/Output	SPI Port MOSI/ GPIO6	SPI Port Master Out Slave In (MOSI) data signal.
29	SPI_MISO	Digital Input/Output	SPI Port MISO / GPIO5	SPI Port Master In Slave Out (MISO) data signal.
30	SPI_SS	Digital Input/Output	SPI Port SS / GPIO4	SPI Port Slave Select (SS) signal.
31	SSI_BITCK	Digital Input/Output	SSI Bit Clock / GPIO3	SSI serial TX/RX clock and is bi-directional.
32	SSI_FSYN	Digital Input/Output	SSI Frame Sync / GPIO2	SSI frame sync for data (RX or TX) and is bi-directional.
33	SSI_RX	Digital Input/Output	SSI RX data input / GPIO1	SSI serial RX data input.
34	SSI_TX	Digital Input/Output	SSI TX data output / GPIO0	SSI serial TX data output.
35	KBI_7	Digital Input/Output	Keyboard Interface Bit 7 / GPIO29	Asynchronous interrupt input.

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description[1]	Functionality
36	KBI_6	Digital Input/Output	Keyboard Interface Bit 6 / GPIO28	Asynchronous interrupt input.
37	KBI_5	Digital Input/Output	Keyboard Interface Bit 5 / GPIO27	Asynchronous interrupt input.
38	KBI_4	Digital Input/Output	Keyboard Interface Bit 4 / GPIO26	Asynchronous interrupt input.
39	KBI_3	Digital Input/Output	Keyboard Interface Bit 3 / GPIO25	Used as output for keyboard interface.
40	KBI_2	Digital Input/Output	Keyboard Interface Bit 2 / GPIO24	Used as output for keyboard interface.
41	KBI_1	Digital Input/Output	Keyboard Interface Bit 1 / GPIO23	Used as output for keyboard interface.
42	KBI_0_HST_WK	Digital Input/Output	Keyboard Interface Bit 0 / HoST Walk-up output / GPIO22	Used as output for keyboard interface / Alternative function as a wake-up output (based on a timer) to external device.
43	COIL_BK	Power Switch Output	Buck converter coil drive output	Onboard buck converter connection to external coil, driven by onboard MOSFET.
44	LREG_BK_FB	Power Input	Voltage input to onboard regulators, buck regulator feedback voltage	• When using onboard buck converter, connect to load side of coil. • When not using buck converter, connect to VBATT.
45	VBATT	Power Input	High side supply voltage to buck regulator switching MOSFET and IO buffers	Connect to battery.
46	RF_PLL_FLT	Analog Voltage	PLL filter connection	• Connection for PLL filter (Type 2, 2nd Order) when using primary crystal with frequency other than 24 MHz (13-26 MHz). • No Connect for 24 MHz crystal.
47	XTAL_32_IN	Analog Input	Optional 32.768 kHz crystal oscillator input	Connect to 32.768 kHz crystal
48	XTAL_32_OUT	Analog Output	Optional 32.768 kHz crystal oscillator output	Connect to 32.768 kHz crystal
49	XTAL_24_OUT	Analog Output	Primary 24 MHz crystal oscillator output	• Connect to 13-26 MHz crystal (24 MHz default). • No load capacitor required • Do not load with any capacitance.
50	XTAL_24_IN	Analog Input	Primary 24 MHz crystal oscillator input	• Connect to 13-26 MHz crystal (24 MHz default). • No load capacitor required • Do not load with any capacitance.
51	RESETB	Digital Input	System reset input	Active low, asynchronous reset
52	TX_ON	Digital Input/Output	Control output for external RF component / GPIO44	Programmable control pin

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description[1]	Functionality
53	PA_NEG	RF Output	RF power amplifier (PA) ouput negative	• Open drain. Must be connected to RF_BIAS through a bias network. • Only used for external dual port operation. • Do not use for single port operation. No Connect.
54	PA_POS	RF Output	RF power amplifier (PA) ouput positive	• Open drain. Must be connected to RF_BIAS through a bias network. • Only used for external dual port operation. • Do not use for single port operation. No Connect.
55	RF_BIAS	Analog Power Output	Analog VDD regulator output	1.5 Vdc voltage regulated output used to supply differential PA output port. When using dual port operation, tie to PA_POS and PA_NEG through bias networks.
56	ANT_1	Digital input / Output	Control output for external RF component / GPIO42	Programmable control pin.
57	ANT_2	Digital input / Output	Control output for external RF component / GPIO43	Programmable control pin.
58	RF_GND	Power Input	RF ground.	Connect to ground VSS.
59	RX_ON	Digital input / Output	Control output for external RF component / GPIO45	Programmable control pin.
60	RF_RX_TX	RF Input/Output	RF single-ended, single port input and ouput	• Interfaces to onboard balun. 50 Ω impedance • Full bidirectional port with onboard T/R switch. • Used as single-ended RF input port for dual port operation with PA_NEG and PA_POS PA outputs.
61	ADC2_VREFL	Analog Input or Digital Input / Output	Low reference voltage for ADC_2 / GPIO39	VREFL for ADC_2.
62	ADC1_VREFL	Analog Input or Digital Input / Output	Low reference voltage for ADC_1 / GPIO41	VREFL for ADC_1.
63	ADC1_VREFH	Analog Input or Digital Input / Output	High reference voltage for ADC_1 / GPIO40	VREFH for ADC_1.
64	ADC2_VREFH	Analog Input or Digital Input / Output	Low reference voltage for ADC_2 / GPIO38	VREFH for ADC_2.
75-79	VSS	Power input	External package GND pads. Common VSS.	Connect to ground.
84-88	VSS	Power input	External package GND pads. Common VSS.	Connect to ground.

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description[1]	Functionality
93-97	VSS	Power input	External package GND pads. Common VSS.	Connect to ground.
102	MDO01	Digital Input/Output	Message Data Out Bit 1 output / GPIO52	Nexus debug port message data output Bit 1.
103	MDO00	Digital Input/Output	Message Data Out Bit 0 output / GPIO51	Nexus debug port message data output Bit 0.
104-106	VSS	Power input	External package GND pads. Common VSS.	Connect to ground.
111	MDO03	Digital Input/Output	Message Data Out Bit 3 output / GPIO54	Nexus debug port message data output Bit 3.
112	MDO02	Digital Input/Output	Message Data Out Bit 2 output / GPIO53	Nexus debug port message data output Bit 2.
113	MSEO1_B	Digital Input/Output	Message Start / End Out Bit 1 output / GPIO60	Nexus debug port message start / end output Bit 1. Signal is active low.
114	MSEO0_B	Digital Input/Output	Message Start / End Out Bit 0 output / GPIO59	Nexus debug port message start / end output Bit 0. Signal is active low.
115	VSS	Power input	External package GND pads. Common VSS.	Connect to ground.
120	MDO05	Digital Input/Output	Message Data Out Bit 5 output / GPIO56	Nexus debug port message data output Bit 5.
121	MDO04	Digital Input/Output	Message Data Out Bit 4 output / GPIO55	Nexus debug port message data output Bit 4.
122	RDY_B	Digital Input/Output	Ready output / GPIO61	Nexus debug port ready output. Signal is active low.
123	EVTO_B	Digital Input/Output	Event Out output / GPIO62	Nexus debug port event out output. Signal is active low.
124	DIG_REG	Digital Power Output	Digital core logic VDD supply.	1.2 Vdc internally regulated VDD supply to digital logic core. No Connect,. For test only
129	MDO07	Digital Input/Output	Message Data Out Bit 7 output / GPIO58	Nexus debug port message data output Bit 7.
130	MDO06	Digital Input/Output	Message Data Out Bit 6 output / GPIO57	Nexus debug port message data output Bit 6.
131	MCKO	Digital Input/Output	Message Clock Out output / GPIO50	Nexus debug port message clock output.
132	EVTI_B	Digital Input/Output	Event In input / GPIO63	Nexus debug port event in input. Signal is active low.

Table 2. Pin Function Description (continued)

Pin #	Pin Name	Type	Description[1]	Functionality
133	NVM_REG	NVM Power Output	FLASH (NVM) VDD supply.	VDD supply to FLASH. Typically No Connect. Can be connected to VDD when regulated 1.8Vdc mode is used.
65-74 80-83 89-92 98-101 107-110 116-119 125-128 134-145	NC		No Connect	These pads are provided for extra mechanical attach strength to meet demanding requirements of drop tests.

1 Pins described as GPIO have an alternative general purpose I/O function.

5.2 Hardware Development Interface Interconnects

The MC13224V supports two development hardware interfaces.

5.2.1 ARM JTAG Interface Connector

The MC13224V supports connection to a subset of the defined ARM JTAG connector. The JTAG hardware interface uses a 20-pin header with a standard 0.1 inch spacing. Table 3 shows how the MC13224V pins are connected to the associated JTAG header pinouts if the JTAG connector is provided on the application.

Table 3. ARM JTAG 20-Pin Connector Assignments

Name[1]	Pin #	Pin #	Name
VBATT	1	2	VBATT
NC[2]	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
RTCK	11	12	GND
TDO	13	14	GND
RESET[3]	15	16	GND
NC	17	18	GND
NC	19	20	GND

1 NC = No Connect.

2 MC13224V does not support separate JTAG reset TRST.

3 VBATT through a 100k-Ω pullup.

5.2.2 Nexus Mictor Interface Connector

The MC13224V also supports connection to a subset of the defined Nexus Mictor connector. The hardware interface is a 38-pin Mictor target connector. Table 4 shows the device pins that are connected to the associated Mictor pin outs if the Mictor connector is used.

Table 4. Nexus 38-Pin Mictor Connector Assignments

Name[1]	Pin #	Pin #	Name
NC	1	2	NC
NC	3	4	NC
NC	5	6	RTCK
NC	7	8	NC
VBATT(pullup)[2]	9	10	EVTI_B
TDO	11	12	VBATT[3]
NC	13	14	RDY_B
TCK	15	16	MDO07
TMS	17	18	MDO06
TDI	19	20	MDO05
RESET[4]	21	22	MDO04
NC	23	24	MDO03
NC	25	26	MDO02
NC	27	28	MDO01
NC	29	30	MDO00
NC	31	32	EVTO_B
NC	33	34	MCKO
NC	35	36	MSEO1_B
NC	37	38	MSEO0_B

1 NC means No Connect.

2 VBATT through a 100k-Ω pullup.

3 VBATT isolated by a 1k-Ω resistor.

4 VBATT through a 100k-Ω pullup.

6 System Electrical Specification

This section details maximum ratings for the 99-pin LGA package and recommended operating conditions, DC characteristics, and AC characteristics.

6.1 LGA Package Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum rating is not guaranteed. Stress beyond the limits specified in Table 5 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{BATT}) or the programmable pull-up resistor associated with the pin is enabled.

Table 5 shows the maximum ratings for the 99-Pin LGA package.

Table 5. LGA Package Maximum Ratings

Rating	Symbol	Value	Unit
Maximum Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	-55 to 125	°C
Moisture Sensitivity Level		MSL3-260	
Reflow Soldering Temperature (for reflow soldering profile and other LGA module reference information, see Freescale Application Note, AN3311)		260	°C
Power Supply Voltage	V_{BATT}, V_{DDINT}	-0.3 to 3.7	Vdc
Digital Input Voltage	Vin	-0.3 to (V_{DDINT} + 0.2)	Vdc
RF Input Power	P_{max}	10	dBm

Note: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

Note: Meets Human Body Model (HBM) = 2 kV. RF input/output pins have no ESD protection.

6.2 Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Operating Voltage Single un-regulated source (VBATT and LREG_BK_FB tied common to V_{DD})	V_{DD}	2.0	-	3.6	Vdc
Onboard buck with un-regulated source (VBATT tied to V_{DD})		2.1	-	3.6	Vdc
Input Frequency	f_{in}	2.405	-	2.480	GHz
Operating Temperature Range	T_A	-40	25	+105	°C
Logic Input Voltage Low	V_{IL}	0	-	30% V_{BATT}	V
Logic Input Voltage High	V_{IH}	70% V_{BATT}	-	V_{BATT}	V
RF Input Power	P_{max}	-	-	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 standard.)	f_{ref}	13	24	26	MHz

6.3 DC Electrical Characteristics

Table 7. DC Electrical Characteristics

(VBATT, LREG_BK_FB = 3.3 V, T_A = 25 °C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage[1] (voltage applied to power input pins; VBATT (pin 45), LREG_BK_FB (pin 44))	V_{DD}	2.0	2.7	3.6	Vdc
High impedance (off-state) leakage current (per pin) (V_{In} = V_{DD} or V_{SS}, all input/outputs, device must not be in low power mode)	$\|I_{OZ}\|$	-	-	1.0	µA
Input Current (V_{IN} = 0 V or V_{DDINT}) (V_{In} = V_{DD} or V_{SS}, all input/outputs, device must not be in low power mode)	I_{IN}	-	-	±1.0	µA
Input Low Voltage (All digital inputs)	V_{IL}	0	-	30% V_{BATT}	V
Input High Voltage (all digital inputs)	V_{IH}	70% V_{BATT}	-	V_{BATT}	V
Input hysteresis (all digital inputs)	V_{hys}	0.06 × V_{DD}		—	V
Internal pullup and pulldown resistors[2] (all port pins and IRQ)	R_{PU}	-	70	-	kohm
Output High Voltage (I_{OH} = -5 mA) (All digital outputs)	V_{OH}	80% V_{BATT}	-	V_{BATT}	V

Table 7. DC Electrical Characteristics (continued)

(VBATT, LREG_BK_FB = 3.3 V, T_A = 25 °C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Low Voltage (I_{OL} = 5 mA) (All digital outputs)	V_{OL}	0	-	20% V_{BATT}	V
Maximum current in/out per IO pin		—		TBD	mA
Maximum total I_{OL} for all IO pins	I_{OLT}	—		TBD	mA
Input capacitance (all non-supply pins)	C_{In}	—	3	—	pF

1 Maximum usable range of the reference voltage supply pin. This range may be modified because of the power supply configuration used in an application. See Table 6, “Power Supply Voltage”.

2 Measurement condition for pull resistors: $V_{IN} = V_{SS}$ for pullup and $V_{IN} = V_{DD}$ for pulldown.

6.4 Supply Current Characteristics

Table 8. Supply Current Characteristics

(VBATT, LREG_BK_FB = 3.3 V, T_A = 25 °C, unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Off current - Device is in reset condition (held in reset) and all GPIO at ground.			0.4	0.6	µA
Hibernate current - RAM retained (8k, 32k, 64k, or 96k) 2KHz onboard oscillator or 32 kHz crystal oscillator CPU off (stop mode) wake-up from RTI timer, or external request Radio off ADCs not available					
8 Kbyte RAM retention			0.9	2.2	µA
32 Kbyte RAM retention			2.3	4.9	µA
64 Kbyte RAM retention			3.7	-	µA
96 Kbyte RAM retention			5.1	-	µA
Doze current - RAM retained (8k, 32k, 64k, or 96k) Onboard 24 MHz oscillator on (high frequency accuracy) CPU off (stop mode) Radio off ADCs available, but inactive					
8 Kbyte RAM retention			55	70	µA
32 Kbyte RAM retention			57	-	µA
64 Kbyte RAM retention			58	-	µA
96 Kbyte RAM retention			60	-	µA
Idle current - All RAM active Reference oscillator on (24 MHz) at 1.2 VDC CPU on at 1 MHz Reference clock available to all peripherals Radio off ADCs available, but inactive			0.85	.95	mA

Table 8. Supply Current Characteristics (continued)

(VBATT, LREG_BK_FB = 3.3 V, T_A = 25 °C, unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Run current - All RAM active Reference oscillator on (24 MHz) at 1.2 VDC CPU on at reference frequency Radio off Reference clock available to all peripherals ADCs available, but inactive			3.3	7.3	mA
Receive current - All RAM active Reference oscillator on (24MHZ) at 1.2 VDC Radio RX on (receiving data) Reference clock available to all peripherals ADC_1 available, but inactive CPU on at 2 MHz (DCD) CPU on at 2 MHz (NCD)			22 24	25 -	mA
Transmit current - All RAM active Reference oscillator on (24MHZ) at 1.2 VDC Radio TX on (sending data @ 0 dBm) Reference clock available to all peripherals ADCs available, but inactive CPU clock at 2 MHz			29	31	mA

6.5 RF AC Electrical Characteristics

Table 9. Receiver AC Electrical Characteristics for 802.15.4 Modulation Mode

(VBATT, LREG_BK_FB = 3.3 V, TA = 25 °C, fref = 24 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Sensitivity for 1% Packet Error Rate (PER)[1] (+25 °C, @ package interface; die sensitivity is ~1dB greater) Non-coherent Differential Chip Detection (DCD) Non-coherent Detection (NCD)		 - -	 -96 -100	 -91 -	dBm
Saturation (maximum input level)	$SENS_{max}$	-	10	-	dBm
Channel Rejection for 1% PER (desired signal -82 dBm) +5 MHz (adjacent channel) -5 MHz (adjacent channel) +10 MHz (alternate channel) -10 MHz (alternate channel) >= 15 MHz		 - - - - -	 38 38 57 57 65	 35 35 50 50 60	dB
Frequency Error Tolerance[2]		200	300	-	kHz
Symbol Rate Error Tolerance[2]		80	120	-	ppm

1 The digital modem contains a block designated as the RX Modem. The Rx Modem can operate in: 1) Non-coherent Differential Chip Detection (DCD) mode which has 3-4dBm less sensitivity but requires 3-4mA less receiver current, and 2) Non-coherent Detection (NCD) mode which has 3-4dBm greater sensitivity but requires 3-4mA greater receiver current.

2 Minimum set by IEEE 802.15.4 Standard

Table 10. Transmitter AC Electrical Characteristics for 802.15.4 Modulation Mode

(VBATT, LREG_BK_FB = 3.3 V, T_A = 25 °C, f_{ref} = 24 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Nominal Output Power[1]	P_{out}	-2	1.5	4.5	dBm
Maximum Output Power[2]		-	+4	-	dBm
Error Vector Magnitude P_{out} @ -30 dBm P_{out} @ 0 dBm P_{out} @ +4 dBm	EVM	 - - -	 13 11 9	 - 20 20	%
Output Power Control Range		-	35	-	dB
Over the Air Data Rate		-	250	-	kbps
2nd Harmonic[3]		-	-55	-	dBm/MHz
3rd Harmonic[3]		-	-64	-	dBm/MHz
Spurious Emissions 30-1000 MHz 1-12.75GHz			 - -		 dB dB
Nominal Impedance (RF_RX_TX)			50		ohm

1 Register sets output power to nominal (0 dBm).

2 Register sets output power to maximum.

3 Measurements taken at output of evaluation circuit set for maximum power out and averaged over 100ms.

Table 11. RF Port Impedance for Dual Port PA Output Pins

Frequency	Symbol	PA_POS (Typ)	PA_NEG (Typ)	Unit
2.405 GHz 2.442 GHz 2.480 GHz	Zout	64.7 - j43.9 64.5 - j42.9 64.3 - j42.0	61.0 - j31.9 60.7 - j30.7 60.4 - j29.5	Ω

6.6 Crystal Reference Clock Oscillator Characteristics

The reference oscillator model including external crystal in shown in Figure 10. The IEEE 802.15.4 Standard requires a frequency tolerance less than or equal to +/- 40 ppm as shown in the oscillator specification Table 12. With a suitable crystal (refer to Table 13 and Freescale Application Note AN3251), the device frequency tolerance can typically trimmed to be held to +/- 30 ppm over all conditions.

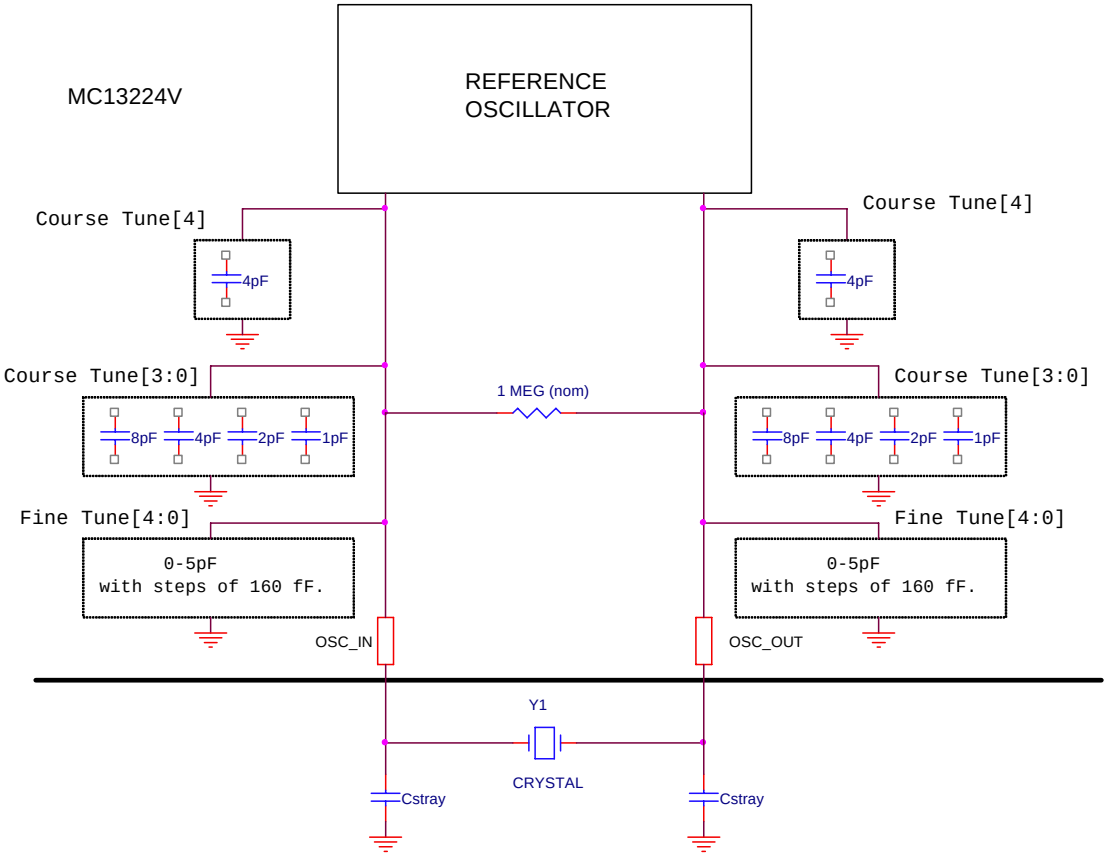


Figure 10. Reference Oscillator Model

Table 12. Reference Oscillator Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency		13	24	26	MHz
Oscillator frequency tolerance over temperature range.			+/- 30	+/- 40	ppm
External load capacitance	C_{Lext}	None required (onboard)			pF
Internal Osc startup time (13 MHz - 26 MHz)[1]			0.8	1.2	ms

1 This is part of device wake-up time.

Table 13. Recommended 24 MHz Crystal Specifications

Parameter	Value	Unit	Condition
Frequency	24.000000	MHz	
Frequency tolerance (cut tolerance)[1]	± 10	ppm	at 25 °C
Frequency stability (temperature drift)	± 15	ppm	Over desired temperature range
Aging	± 2	ppm	max
Equivalent series resistance[2]	40-50	Ω	max
Load capacitance	5 - 9	pF	
Shunt capacitance	<2	pF	max
Mode of oscillation			fundamental

1 A wider frequency tolerance may acceptable if application uses trimming at production final test.

2 The higher ESR may be acceptable with lower load capacitance.

6.7 Optional 32.768 KHz Crystal Oscillator Specifications

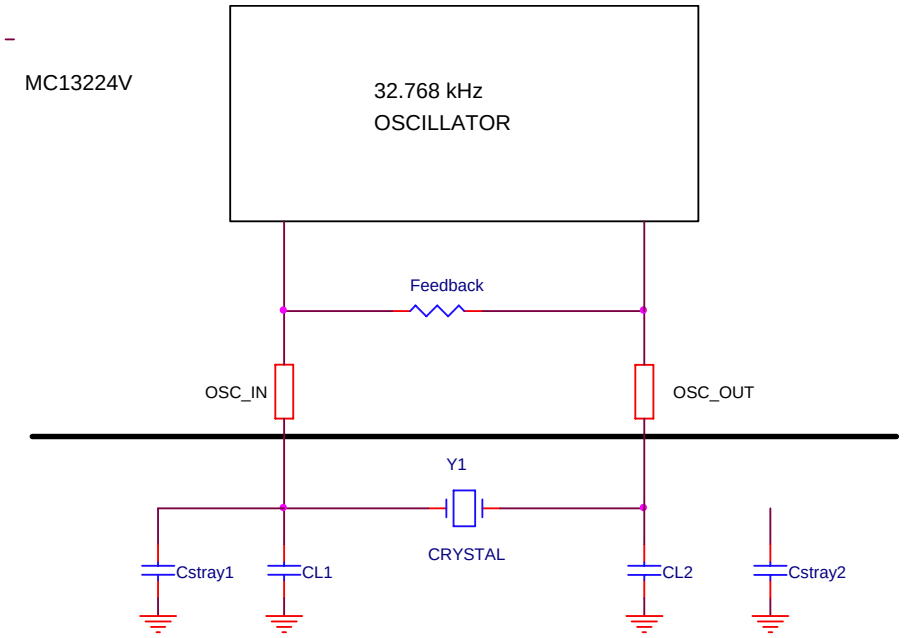


Figure 11. 32.768 KHz Oscillator Mode

Table 14. 32.768 Oscillator Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal frequency[1]			32.768		KHz
Frequency tolerance @ 25 °C			± 20		ppm
Frequency tolerance over temperature[2]			-0.034 ±0.006ppm / (25-T)[2]		ppm

Table 14. 32.768 Oscillator Specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Load capacitance		11	12.5	13	pF
Equivalent series resistance (ESR)				60	kΩ
Shunt capacitance				1.35	pF
Tolerated drive level				1	μW

1 Recommended crystal Abracom Corporation crystal part number ABS25-32.768-12.5-B

2 Example; Stability at -20×C is: -0.034 x (25-[-20])^2= -68.8ppm.

6.8 Internal Low Speed Reference Oscillator Specifications

Table 15. Internal 2 KHz Oscillator Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Default Frequency @ 25 °C		2.5	1.7	3.5	KHz
Oscillator frequency variation over full temperature range		-	+/- 13	-	%
Calibration time (in terms of 2KHz osc clocks)		-	-	2^{16}-1	osc clks

6.9 Control Timing and CPU Bus Specifications

Table 16. MCU Control Timing

(VBATT, LREG_BK_FB = 3.3 V, T_A = 25 °C, f_{ref} = 24 MHz, unless otherwise noted.)

Parameter	Symbol	Min	Typical	Max	Unit
CPU Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	f_{ref}/64 [1]	—	f_{ref} [1]	MHz
CPU Bus frequency with active TX or RX		2			MHz
Real-time interrupt internal oscillator frequency			2		KHz
External reset pulse width[2]		-	4	—	osc clks
External minimum interrupt pulse width (KBI[7:4])		-	4	—	osc clks

1 Normal operation uses a 24 MHz reference. The MC13224V allows up to a 26 MHz max reference oscillator.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. There always must be 3 clocks of the operating oscillator; this can vary from the low power oscillators to the reference oscillator.

6.9.1 Timer Module Input Characteristics

Four-bit synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the peripheral clock rate. Table 17 shows timer input timing values.

Table 17. Timer Input Timing

(VBATT, LREG_BK_FB = 3.3 V, TA = 25 °C, fref = 24 MHz, unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
External clock frequency		dc	peripheral_bus_clk/3	MHz
External clock period		>3	—	t_{cyc}
Input capture pulse width		>3	—	t_{cyc}

6.10 SPI Timing

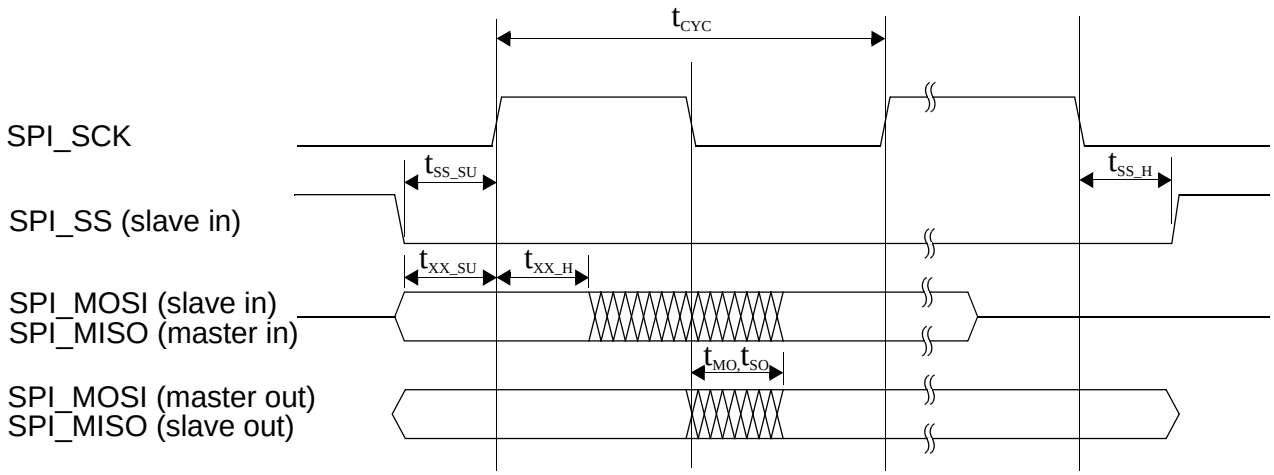


Figure 12. SPI Timing Diagram

Table 18 describes the timing requirements for the SPI system.

Table 18. SPI Timing

Parameter	Symbol	Min	Typical	Max	Unit
Master SPI_SCK Period	t_{CYC}	peripheral_ Clk*2	38	peripheral_ Clk *256	ns
Slave SPI_SCK Period	t_{CYC}	10			ns
Slave SPI_SS Setup Time	t_{SS_SU}	10			ns
Slave SPI_SS Hold Time	t_{SS_H}	10			ns
Slave SPI_MOSI Setup Time	t_{SI_SU}	10			ns
Slave SPI_MOSI Hold Time	t_{SI_H}	10			ns
Master SPI_MISO Setup Time	t_{MI_SU}	20			ns
Master SPI_MISO Hold Time	t_{MI_H}	0			ns
Master SPI_MOSI Output Time	t_{MO}			5	ns
Slave SPI_MISO Output Time (with 15 pf load)	t_{SO}			20	ns

6.11 I²C Specifications

Table 19 describes the timing requirements for the I²C system.

The I²C module is driven by the peripheral bus clock (typically max 24 MHz) and the SCL bit clock is generated from a prescaler. The prescaler divide ratio can be programmed from 61,440 to 160 (decimal) which gives a maximum bit clock of 150 kbps.

Table 19. I²C Signal DC Specifications (I2C_SDA and I2C_SCL)

Parameter	Symbol	Min	Typical	Max	Unit
Input Low Voltage	V_{IL}	-0.3	-	0.3 V_{DDINT}	V
Input High Voltage	V_{IH}	0.7 VBATT	-	VBATT + 0.3	V
Input hysteresis	V_{hys}	0.06 × VBATT		—	V
Output Low Voltage[1] (I_{OL} = 5 mA)	V_{OL}	0	-	0.2 VBATT	V
Input Current (V_{IN} = 0 V or V_{DDINT})	I_{IN}	-	-	±1	µA
Pin capacitance	C_{in}			<10	pF

1 SDA and SCL are open drain outputs

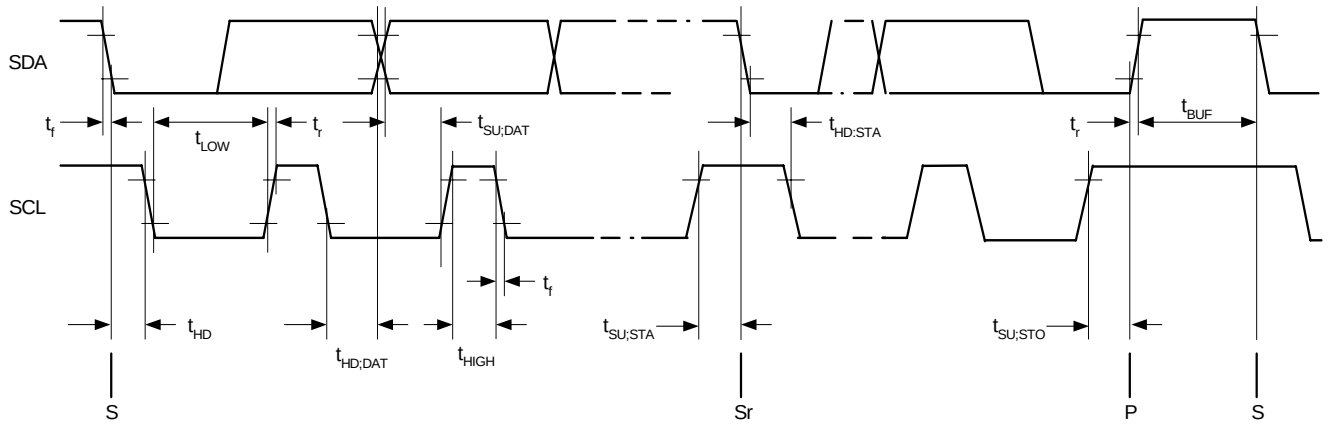


Figure 13. I²C Timing Diagram

NOTE

The I²C timing limits reflect values that are necessary meet to the I²C Bus specification.

Table 20. I²C Signal AC Specifications[1]

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency (when source)	f_{SCL}	0	100	0	150	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time	$t_{SHD;DAT}$	0[2]	3.45[3]	0[2]	0.9[3]	µs
Data setup time	$t_{SU:DAT}$	250	-	100[4]	-	ns
Rise time for both SDA and SCL signals	t_r	-	1000	$20 + 0.1C_b$[5]	300	ns
Fall time for both SDA and SCL signals	t_f	-	300	$20 + 0.1C_b$[5]	300	ns
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF

1 All values referred to V_{IHmin} and V_{ILmax} levels

2 A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3 The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

4 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{SU;DAT} >= 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\ max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

5 C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, the faster fall-times are allowed.

6.12 FLASH Specifications

Table 21. FLASH Characteristics

(TA = 25 °C, fref = 24 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage for program/erase/read (with directly regulated supply)	$V_{prog/erase}$	1.70		1.90	V
SPI clock frequency	f_{FCLK}			13	MHz
Read current (13 MHz)			9	15	mA
Program and erase current			10	15	mA
Standby current			2	10	μA
Sector erase duration				75	ms
Block erase duration				75	ms
Chip erase duration				150	ms
Byte program duration				60	μs
Program/erase endurance		100,000			cycles
Data retention	t_{D_ret}	100		—	years

6.13 ADC Characteristics

Table 22. ADC Electrical Characteristics (Operating)

(VBATT, LREG_BK_FB = 3.3 V, TA = 25 °C, fref = 24 MHz, unless otherwise noted.)

Characteristic	Condition	Symbol	Min	Typical	Max	Unit
ADC supply current (per ADC)	Enabled		—	2.9	6	mA
	Disabled		—	5	-	μA
Reference potential, low		V_{REFL}	VSS	—	V_{REFH}	V
Reference potential, high		V_{REFH}	V_{REFL}	—	VBATT	V
Analog input voltage[1]		V_{INDC}	V_{SS} – 0.2	—	V_{DD} +0.2	V
“Battery” input channel reference voltage				1.2		V

[1] Maximum electrical operating range, not valid conversion range.

Table 23. ADC Timing/Performance Characteristics

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Resolution				-	12	Bits
Effective Resolution				8		Bits
Number of input channels					8	
ADC conversion clock frequency	f_{ADCCLK}		-	-	300	KHz
Conversion cycles (continuous convert)	CCP			6		ADCCLK cycles
Conversion time	T_{conv}		20	—	-	µs
Input Leakage Current			—	—	-	nA
Analog Input Voltage[1]	V_{AIN}	VDD	V_{REFL}		V_{REFH}	V

[1] Analog input must be between V_{REFL} + 0.2 and V_{REFH} - 0.2 for valid conversion.

7 Developer Environment

The MC1322x family is supported by a full set of hardware/software evaluation and development tools.

7.1 Hardware Development Interfaces

The ARM debug environment supports both a JTAG debug interface and an extended capability Nexus interface.

7.1.1 JTAG Hardware Debug Port

The JTAG port is the simpler and more common debug port for the ARM core. A standard 20-pin connector as described in Section 5.2.1, “ARM JTAG Interface Connector””, is connected to the TDI, TMS, TCK, TDO, and RTCK signals of the MC13224V. Through the JTAG serial interface, standard debug and development activities such as accessing memory and registers, control of the CPU, download of FLASH memory, and software debug can be accomplished.

7.1.2 A7S Nexus3 (NEX) ARM7 Core Development Interface

The development and debug environment of the ARM7TDMI-S core is based on the A7S Nexus3 interface (compliant with a Class 3 device of the IEEE-ISTO 5001 standard for real-time embedded system design). This interface allows expansion of the development features of the JTAG port (through the addition of auxiliary signals, see Section 5.2.2, “Nexus Mictor Interface Connector”). Development features include:

- Program Trace via Branch Trace Messaging (BTM). Branch trace messaging displays program flow discontinuities (direct and indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus static code may be traced.

- Data Trace via Data Write Messaging (DWM) and Data Read Messaging (DRM). This provides the capability for the development tool to trace reads and/or writes to (selected) internal memory resources.
- Ownership Trace via Ownership Trace Messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An Ownership Trace Message is transmitted when a new process/task is activated, allowing the development tool to trace ownership flow.
- Run-time access to the memory map via the JTAG port. This allows for enhanced download/upload capabilities
- Watchpoint Messaging (WPM) via the auxiliary pins
- Watchpoint Trigger enable of Program and/or Data Trace Messaging
- Auxiliary interface for higher data input/output
- Registers for Program Trace, Ownership Trace, Watchpoint Trigger, and Read/Write Access
- Programmable processor stall function to mitigate message queue overrun risk
- All features controllable and configurable via the JTAG port

7.2 Software Development Tools

An Integrated Development Environment (IDE) is available to facilitate the development of embedded applications targeting the MC13224V platform. Features of the IDE include:

- Project management tools and code editor
- Highly optimizing ARM compiler supporting C and C++
- Extensive JTAG and RDI debugger support
- Run-time libraries including source code
- Relocating ARM assembler
- Linker and librarian tools
- Debugger with ARM simulator, JTAG support and support for RTOS-aware debugging on hardware
- RTOS plug-ins available
- Code templates for commonly used code constructs
- Sample projects for evaluation boards
- User and reference guides, both printed and in PDF format
- Context-sensitive online help

The IDE is complemented by the BeeKit™ Wireless Connectivity Toolkit. BeeKit is a stand alone software application targeting Windows® operating systems. BeeKit provides a graphical user interface (GUI) in which users can create, modify, save, and update wireless networking solutions. With the solution explorer property list windows, users can set configuration parameters to control the setup and execution behavior of the wireless link within their application. The configuration parameters can be validated inside BeeKit to ensure all values provided are within acceptable ranges prior to generation of a workspace. All this functionality provides a mechanism for developers to configure and validate their network parameters

without having to navigate through multiple source files to configure the same parameters. BeeKit supports Freescale's Simple MAC (SMAC), IEEE 802.15.4-compliant MAC, and the Freescale BeeStack™.

7.3 Development Hardware

Several different development modules and kits will be available to allow evaluation of ZigBee and IEEE 802.15.4 applications. The modules will provide capabilities for Coordinator, Router, and End Device nodes. Reference designs will be available for RF design and low power applications including 2-layer and 4-layer PCBs.

8 Mechanical Diagrams (Case 1901-01, non-JEDEC)

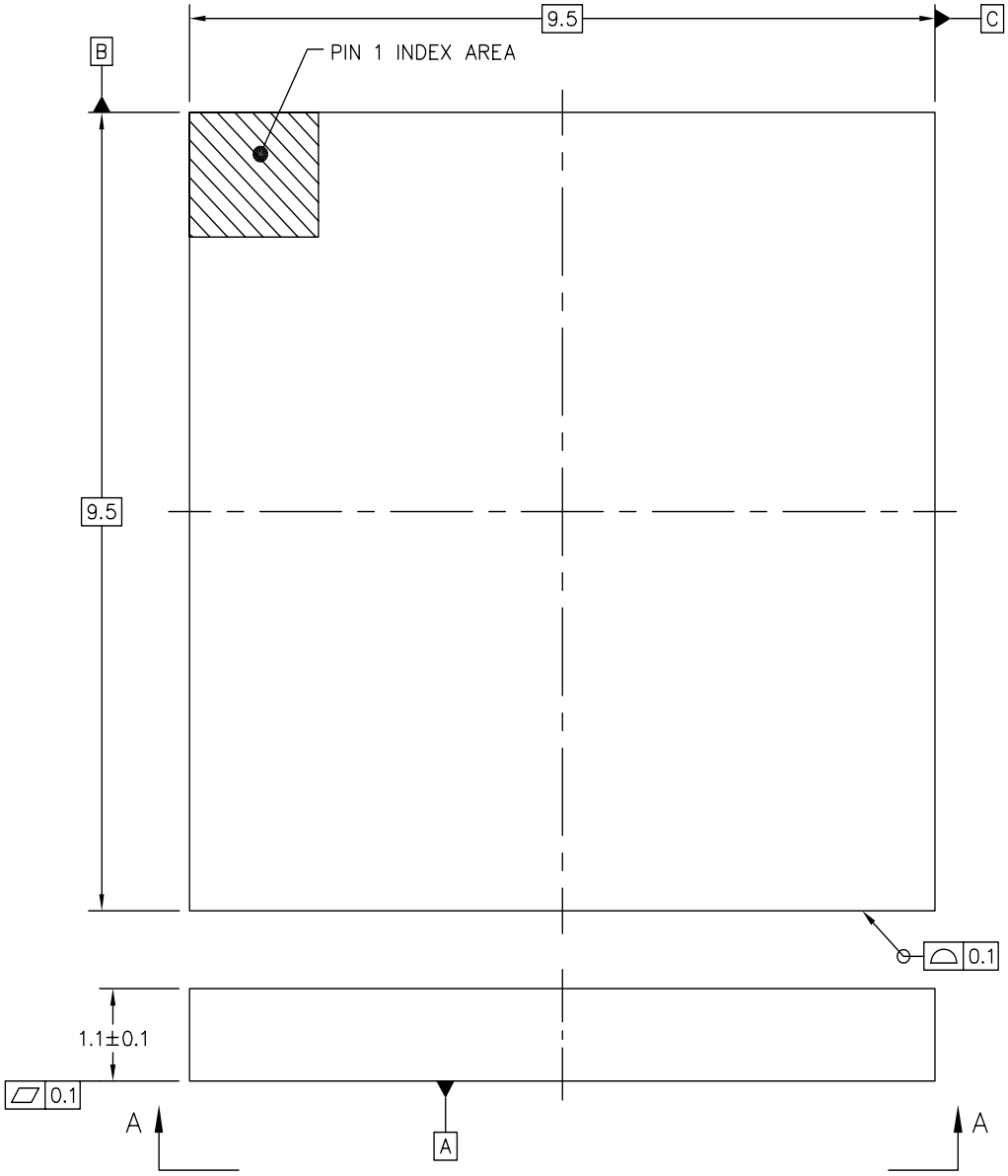


Figure 14. Mechanical Diagram (1 of 2)

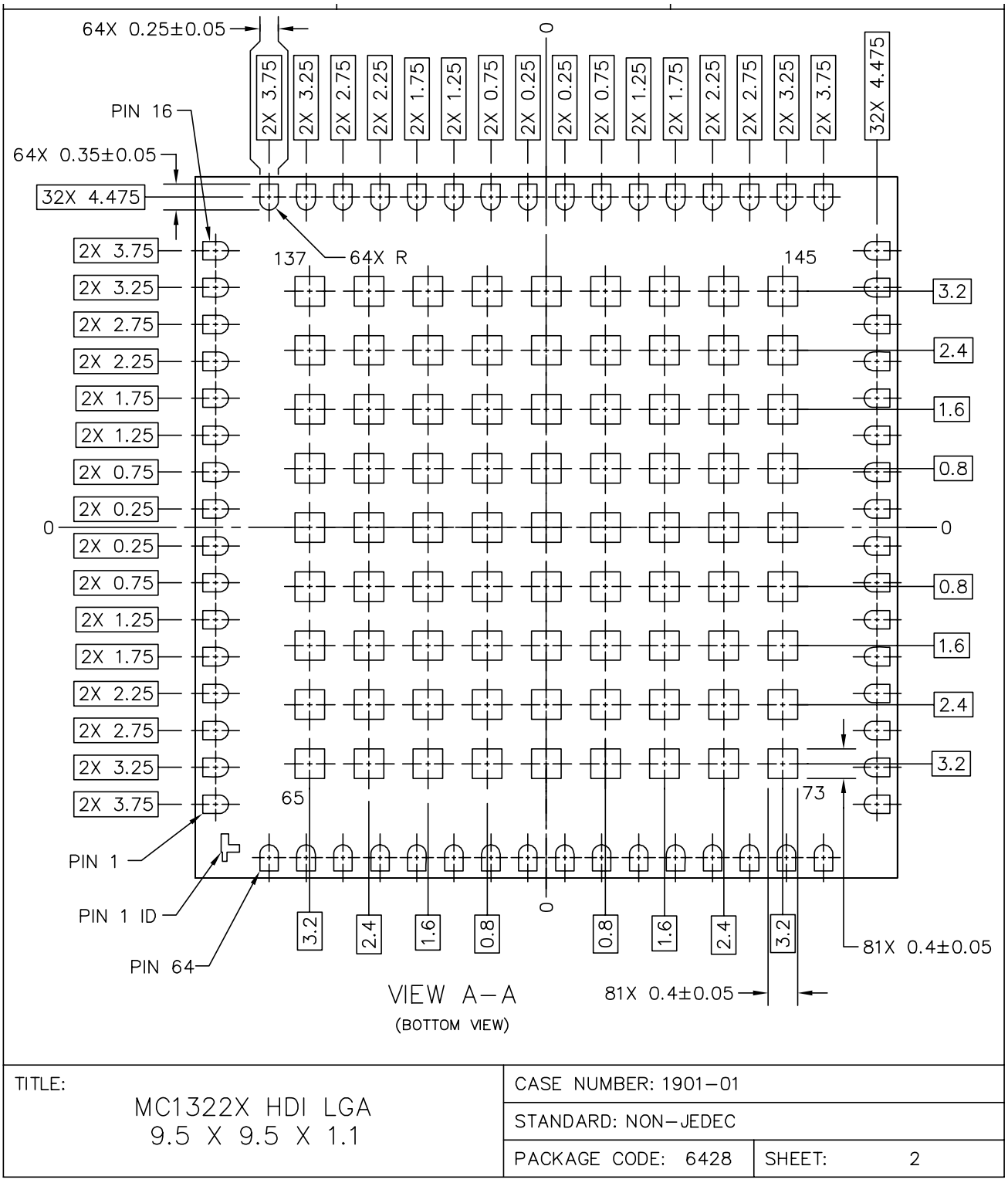


Figure 15. Mechanical Diagram Bottom View (2 of 2)

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